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PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

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TITLE OF THE INVENTION (500 characters max)

METHODS FOR FABRICATION OF POSITIONAL and COMPOSITIONALLY CONTROLLED NANOSTRUCTURES ON SUBSTRATES

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Respectfully submitted,

SIGNATURE C R Nold

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PROVISIONAL APPLICATION COVER SHEET
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METHODS FOR FABRICATION OF POSITIONAL AND COMPOSITIONALLY CONTROLLED NANOSTRUCTURES ON SUBSTRATES

CROSS-REFERENCE TO RELATED APPLICATIONS

None

STATEMENT OF GOVERNMENTAL SUPPORT

This invention was made during work supported by U.S. Department of Energy under Contract No. DE-AC03-76SF00098. The government has certain rights in this invention.

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention describes methods for patterning a substrate to create positional and compositionally well defined nanostructures and nanostructure arrays on a wafer scale. The patterned nanostructures have applications in biological and chemical sensing, catalysis, nanocomputing and nanoelectronics.

RELATED ART

Nanostructures are structures with characteristic dimensions less than 100nm, i.e. nanoscale. Matters can exhibit size dependent properties at this scale due to physical laws governing microscopic objects, which enable novel applications. Despite their novel property,

however, an economic and production worthy method of fabricating nanostructures and nanostructure arrays on substrate and making necessary connections for functional devices has yet to be found.

Methods for fabricating nanostructures on substrate fall into two categories, top-down and bottom-up approaches. Conventional top-down approaches such as photolithography, electron beam lithography or ion beam lithography involve creating structures by forming and removing unwanted parts of various films. They are prohibitively expensive for forming devices less than 100nm. The resolution of photolithography also suffers from the physical limit of the wavelength of the electromagnetic radiation. Although 30 nm resolution has been demonstrated with extremely short electromagnetic radiation, the cost of such a tool is prohibitively expensive. Electron beam lithography and ion beam lithography boast better resolution down to 10 nm, but these methods require the energetic particle beam to visit each spot sequentially and greatly limit the number of devices that can be made in an industrial production environment.

Other novel lithography methods have emerged over the years. Direct write approaches use scanning probe microscopy to deposit molecules on or change physical or chemical properties of the substrate in the proximity of the probe. These methods suffer from slow speed and lack of a general applicability to fabricate functional devices, which limit their use for industrial production.

Imprint lithography is known in the art whereby a mold with nanostructures is pressed into a thin polymer film on a substrate, which retains the thickness contrast relief pattern after removal of the mold. Further process is then used to transfer the pattern into the whole resist. However, imprint lithography does not generate a pattern; it only transfers an existing pattern on the mold. To generate the nanostructure pattern on the mold, another lithography method is

required, preferably electron beam lithography. This limitation makes the mold fabrication very expensive and imprint mold made today has very low surface coverage of nanostructure-patterned area.

In bottom-up approaches, nanoscale building blocks are synthesized initially by chemical methods, then selectively added to (rather than removal from) a substrate, followed by making contacts to make a functional device. However, these approaches have limitations on the degree of control they can achieve on each stage of the device fabrication and are not suitable for industrial production.

Nanoscale building blocks that can be chemically synthesized include carbon annotate, nanowire, nanocrystal, nanorod, etc. Most of the synthesis processes produce a multitude of nanoscale products, which have different dimension, composition and shape, therefore, different physical and chemical properties. For example, heterogeneous nanowires synthesized by chemical vapor deposition are shown in *Chem. Mater.* 2000, v12, p605 – 607 (Wu,Y. and Yang, P.). To control the diameter, researchers control the diameter of the catalyst used to grow them, which only shifts the center of a broad distribution of the diameters of materials synthesized, as shown in FIG 2 of *Appl. Phys. Lett.* 2001, v78, p2214. To dope the nanowires, investigators introduce gases containing the dopant during the synthesis, as in *J. Phys. Chem.* 2000, v104, p5213. Although no reproducibility is reported, the uniformity of doping is not expected to be good due to the difference in growth rate related to the broad diameter distribution of nanowires.

Assembly of a nanostructure device by depositing building blocks on a substrate for further processing is currently done by liquid assisted methods, such as Langmuir-Blodgett film or fluidic alignment through micromolded channels. They are described in *Nano Letters*, 2003, v3, p1255, *Science*, 2001, v291, p630, *Science*, 2001, v291, p851. These prior art methods suffer

from the fact that they can not achieve the degree of position control the modern semiconductor industry has down to 0.01 μm, as shown in FIGs 2 and 4 of *Science* 2001, v291, p630, where broken, double, and tilted lines are seen. The positions are not highly controlled. Another drawback for these methods is that it is still experimental and has a difficult time to scale up for production.

The final step in making nanostructures into a functional device usually requires an electrical connection to a signal processing unit. The lack of positional control in the bottom-up approach in depositing the nanostructures on the substrate makes the final connection-making step difficult. Often the position of each nanostructure has to be determined by microscopy methods such as scanning electron microscopy or atomic force microscopy; then electron beam lithography or other serial lithography is used to make the connections. Or alternatively, preexisting contact structures are fabricated with top-down methods; nanoscale building blocks are then deposited onto these structures with contacts established by chance. Although small quantities of samples have been built using these techniques for lab studies, they are not suitable for large-scale manufacturing.

To address this problem, a novel method is invented to produce high-density nanowire arrays, *Science*, v300, p 112. Although this method eliminated the nanowire synthesis step and the assembly step, since they have control over the nanowire position, it is still not a production-worthy method on the industrial scale. The method relies on the selective removal of AlGaAs in the AlGaAs/GaAs superlattice, and uses the superlattice as a mold to deposit materials on wafer. The area that can be patterned is defined by the superlattice thickness; to grow a superlattice up to 100 μm is a very time-consuming step. Even so, they can only pattern a 100-μm area at the

most, and thus exhibit a slow throughput process. The method is also limited to produce only straight nanowire patterns, and not any other shapes.

Sidewall image transfer (SIT) was invented by the semiconductor industry in early 1980s to produce sublithography images and spaces for the formation of polysilicon gate in sub-micron range. Briefly, a vertical step is created on a planar substrate, which is covered by conformal deposition of a silicon oxide, preferably silicon dioxide or nitride. The resulting gate length is approximately equal to the thickness of the layer deposited. More details can be found in US patent 4,358,340, 4,419,809, 4,419,810, 5,139,904, and 5,795,830. A more recent application of this method is towards the fabrication of FinFET, as disclosed in *IEEE Device Letters*, 2002, v23, p25 and *Solid-State Electronics*, 2002, v46, p1595, the contents of which are hereby incorporated by reference in its entirety for all purposes.

Despite its ability to create sublithography patterns, SIT has only been applied to specific materials, namely Si and polysilicon, and to specific devices such as transistors. The minimum feature dimension can be achieved by this method is on the order of 20nm and thus limits its application in creating nanostructures.

A need exists for methods that can fabricate positional, compositionally and shape controlled nanostructures and nanostructure arrays on a substrate to enable large-scale manufacturing.

Imprint lithography can transfer nanoscale patterns on a large area, but it can not generate patterns. Existing methods for fabrication of nanostructures with imprint lithography depend on electron beam lithography to make the nanoscale patterns in a mold, which can be very expensive for mold with high nanoscale pattern coverage. The present invention contemplates

that nanoscale patterns can be made on a substrate, which can then be used as mold in imprint lithography.

Nanowire biosensors have been discussed in the literature, *Science* 2001, v293, p1289 and *Nano Letters*, 2004, v4, p51, the content so both are hereby incorporated by reference in its entirety. These sensors are assembled from CVD-synthesized nanowires, and they are difficult to manufacture on an industrial scale. Sensors of the prior art do not have the compositional and positional control over the nanostructures that arrays and sensors made in accordance with the present invention possess. In general, the sensors include nanotubes or nanowires in contact with electrodes, thus forming a circuit for current flow. The sensing occurs when analytes contact the nanotubes or nanowires. Chemical sensors based on TiO_2 nanowire are also reported. The present invention contemplates that nanoscale sensing devices may be manufactured cheaply in mass.

SUMMARY OF THE INVENTION

In accordance with one aspect of the present invention, a method for fabricating positional and compositionally controlled nanostructures is disclosed. In one embodiment the method comprises:

(a) forming a nanoscale thin film of desired nanostructure material composition on the substrate and optionally covering it with a protective layer;

(b) forming a sacrificial layer on top of the protective layer and patterning the sacrificial layer by conventional or advanced lithography;

(c) depositing a thin conformal layer over the patterned sacrificial structure which has different etching characteristics than the sacrificial layer;

(d) anisotropically etching the conformal layer to expose the sacrificial layer and removing the sacrificial layer by selective etching;

(e) transferring the resulting conformal layer structure through the protective layer to the nanoscale thin film of desired material by etching, and removing the remaining conformal layer structure and protective layer;

(f) depending on application, the resulting nanostructures in the thin film can be further reduced in dimension by controlled etching or converting to a material that has different etching characteristics and removing the material through selective etching;

(g) depending on application, the shape of the nanostructure can be modified by standard lithography and etching to remove unwanted parts of the above fabricated nanostructures.

In accordance with another aspect of the invention, a method for fabricating positional and compositionally controlled arbitrary shape nanostructures on a substrate is provided. In one embodiment the method comprises:

(a) optionally forming a protective layer on a substrate;

(b) forming a sacrificial layer on top of the protective layer and patterning the sacrificial layer by conventional or advanced lithography;

(c) depositing a thin conformal layer over the patterned sacrificial structure which has different etching characteristics than the sacrificial layer;

(d) anisotropically etching the conformal layer to expose the sacrificial layer and removing the sacrificial layer by selective etching;

(e) transferring the resulting conformal layer structure through the protective layer to the nanoscale thin film of desired material by etching, and removing the remaining conformal layer structure and protective layer;

(f) depending on application, the resulting nanostructure pattern in substrate can be further reduced in dimension by controlled etching or converting to a material that has different etching characteristics and removing the material through selective etching;

(h) depending on application, the shape of the nanostructure can be modified by standard lithography and etching to remove unwanted parts of the above fabricated nanostructures.

(g) the above nanostructure pattern in substrate then can be used as mold in imprint lithography and create positional and compositionally controlled nanostructures by a lift-off process or an etching process, both of which are well-known in semiconductor industry.

The above fabrication methods, as employed herein, can create at least one nanoscale pattern, a multiple of patterns, of specific predetermined position, shape and composition, patterns over a large area at high throughput satisfactory for industrial requirement. The resultant nanostructure patterns are useful for nanostructure arrays, specifically sensor and catalytic arrays.

In one embodiment, the fabrication process of a nanoscale semiconductor sensor array for detecting analytes is provided, with preferred applications in chemical and biological sensing. Two conductive elements connect the nanostructures to a signal control and processing unit. In one arrangement, the conductive elements are fabricated within the said thin semiconductor

layer, see FIG 5d ref. num 15. In another arrangement, the conductive elements are formed on the nanostructure using standard lithography, see FIG 5f num 19. In some arrangements, sections of the nanostructure can be suspended from the substrate. The said nanostructure semiconductor then can be functionalized with specific molecules for detection of certain molecules.

In another embodiment, the fabrication method of a nanoscale oxide sensor array for detecting analytes is provided, with preferred applications in gas phase sensing. A mold with nanostructure features is fabricated by the second method, and is pressed against a substrate coated with a polymer resist to transfer pattern. Upon separation, the pattern is transferred all the way through the resist by etching. In one arrangement, the desired composition of materials is then deposited on the resist layer. When the resist is dissolved in solution, nanostructures with desired composition are left on the substrate. In another arrangement, a masking material is deposited on the resist layer. Following the dissolution of the resist layer, the masking material that is left on the semiconductor surface can then be used to transfer the nanostructure pattern into the substrate. Two conductive elements can be made to each of the nanostructures by standard lithography methods.

A method for detecting analytes is also provided. The resistance of each of the sensor elements in the sensor arrays fabricated by the two said methods is measured before and after exposure of the sensor arrays to a sensing environment. Resistance change of each of the sensor elements is then correlated to the detection of the specific analyte the sensor is designed to measure. Optimizing the sensor design by control of the dimension, shape and composition can lead to detection at very low levels, i.e. and ppt concentrations.

Future features and advantages of the present invention will become apparent to those of ordinary skills in the art in view of the detailed description of preferred embodiments below, when considered together with the attached drawings and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG 1a- 1b is a block diagram for forming an array in accordance with one embodiment of this invention

FIG 2 is a schematic drawing of a size reduction lithography process in accordance with one embodiment of the present invention.

FIG 3a is a SEM of a cross section of an array after thin LTO deposition (44nm)

FIG 3b is a SEM of a cross section of an array after thick LTO deposition (200 nm).

FIG 3c is a SEM of a cross section of an array after the top LTO layer and poly-Si layer have been etched away from the structure

FIG 3d is a SEM of a cross section after the top LTO layer and poly-Si have been etched away from the structure.

FIG 3e is a SEM cross section of a 20-nm Si nanostructure array made from size reduction lithography

FIG 3f is a SEM to view of the 20-nm Si nanostructure array of FIG 2e.

FIG 4a is SEM cross section of a 12-nm Si nanostructure array made after thermal oxide trimming. Inset HRTEM image shows the single crystalline nature of the Si nanowire.

FIG 4b is a SEM cross section of a 7-nm Si nanostructure array made after further thermal oxide trimming.

FIG 5a-5g is a block diagram of a method in accordance with one embodiment of the present invention.

FIG 6a-6d is a block diagram of a method in accordance with one embodiment of the present invention. Fig 6b shows closed ended nanostructures, FIG 6d shows open ended nanostructures.

FIG 7a-7f is a block diagram of a method in accordance with one embodiment of the present invention.

FIG 8a-8e is a method in accordance with one embodiment of the present invention utilizing imprint lithography.

FIG 9a-9g is a block diagram of a method in accordance with one embodiment of the present invention.

FIG 10a-10b is a depiction of an array and sensor in accordance with one embodiment of the present invention.

FIG 11 is a method in accordance with one embodiment of the present invention.

FIG 12 is a method in accordance with one embodiment of the present invention.

FIG 13 is a method in accordance with one embodiment of the present invention.

FIG 14 is a method in accordance with one embodiment of the present invention.

FIG 15 is a method in accordance with one embodiment of the present invention.

FIG 16 is a method in accordance with one embodiment of the present invention.

FIG 17 is a method in accordance with one embodiment of the present invention.

FIG 18 is a method in accordance with one embodiment of the present invention.

FIG 19 is a method in accordance with one embodiment of the present invention.

FIG 20 shows an embodiment of a suspended nanostructure.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT

By "substrate" it is meant a layer or layers of materials on which the nanostructure array can be fabricated. The substrate may be a single layer of Si, preferably as pure as possible, preferably at least 99.9 % pure. The substrate may be transparent (as for use in an optoelectronic device) or opaque. Generally the thickness of the substrate, whether it is one or multiple layers, is between 500 nm and 1mm, but this can vary depending on the intended use.

Silicon is a preferred material for the substrate. However, also contemplated as materials include SiO_2, Group II-VI and Group III-V semiconductors, any glass or quartz, sapphire, polished metals providing they have an insulating coating. The wafer size may be any size depending on the manufacturing parameters. For the purpose of fabricating a functional device, it is to be understood that the substrate preferably has either have an insulator material thereon, or the substrate comprises an insulator, such as SiO_2, Al_2O_3 or other insulating material. Oxides are preferred because they are capable of processing at high temperatures. The insulating layer may be grown, deposited by any CVD technique, sputtering or evaporation or ion implantation.

By "SOI" it is meant "silicon on insulator". This is a substrate comprising multiple layers, that Si/insulator/Si. The top layer and bottom layer may be substituted for other materials as described herein, for the present invention. A preferred thickness for SOI substrate is between 500-700 μm. The thickness for the oxide layer here, and for insulator layers used herein in general ranges from between 5nm to about 100 μm; preferred thickness is 50 nm to 100 nm. The thickness of the single crystal Si layer ranges from 0.5 nm to about 500 nm; preferred thickness is 5 nm to 50nm.

By "polysilicon" it is meant a contraction of "polycrystalline silicon".

By "silicon oxide, silicon nitride" it is meant all stoichiometric ratios of the compounds.

By "forming a nanoscale thin film" it is meant to include the process of providing a substrate and growing, depositing , bonding or otherwise providing materials in the film format. The film thickness can range from 0.5 nm to 500 nm, preferred thickness is 5nm to 100 nm. The materials can be conductor, semiconductor or insulator in single crystal, polycrystalline or amorphous state. Preferably, it is single crystal Si. Ge or other semiconducting materials may also be used. Si_xGe_{1-x}, where $.01 \leq x \leq .99$, where x is mol % are also contemplated. Conducting polymers known in the art are also contemplated. The film can also comprise more than one layer of materials, with materials for each layer chosen from the above-mentioned materials.

By "thin conformal layer" it is meant a layer having a thickness from about 1nm to about 1μm, depending on the desired end product. Preferably the thickness is less than about 50 nm. Methods for forming a conformal layer include, but are not limited to chemical vapor deposition, spin coating or by converting the underlying layer through chemical reaction such as oxidation or nitrification and low pressure chemical vapor deposition, etc.

By "nanostructure" is meant that at least one, preferably two, of the structure's three dimensions is measured in nanometers. The height and width of the nanostructures in accordance with preferred embodiments of the present invention are between about .5 and 100nm, preferably between 5-50 nm.

By "array" it is meant a substrate having at least one nanostructure thereon.

By "anisotropically etching" it is mean removing material with one preferred direction . Preferred methods for performing anisotropic etching are based on plasma etching.

By "positional controlled" it is meant the ability to fabricate a nanostructure on a substrate and control the placement of the nanostructure within about 20 nm or less. The predetermined position for a nanostructure is determined by the selection of any desired specific

location on a wafer from any particular or specific point on the nanostructure or nanostructures. Positional control also means different nanostructures may be fabricated having a specific predetermined location on the wafer with respect to one another or others.

By "photolithography" it is meant lithographic techniques using any wavelength, including extreme UV.

By "compositionally controlled" it is meant that the method of the present invention is capable of fabricating nanostructures having any material, compositions and stoichiometric ratios thereof, including multiple layers vertically. The present invention contemplates that as many as 100 layer or more can be in 1 nanostructure.

By "etching characteristic" it is meant etching selectivity.

By "pattern" it is meant a design of specific intention that carries with it a specific shape which may include circular, corrugated, elliptical, oblong, oval, parabolic, rectangular and segments or parts of the aforementioned shapes. Complex shapes are also possible, limited only by the imagination. The pattern may be continuous or discontinuous. The thickness or width of the pattern nanostructure does not have to be uniform, but may vary. The height of the pattern may change. FIG 3f shows an example of a pattern in accordance with one embodiment of the present invention.

By "detecting" it is meant that meaning which is associated in the art with this term, such as observe, find, discover, notice, discover or determine the existence, presence, change or any other condition or state.

By "at least one nanostructure in the top layer" it is meant that the nanostructure is structurally integral with the top layer. This means, that the top layer is the nanostructure. The

nanostructure was made from the top layer of a substrate, for example SOI, where the silicon was the top layer initially, and in the top layer everything but the nanostructure has been etched away.

By "insulating layer" it is meant materials capable of insulating electrical current flow from the device. Typically, metal oxides are used. Preferred for use in this invention are SiOx, where $.5 \leq x \leq 2$.

By "predetermined position" it is meant that the nanostructures are positioned on the substrate with precision and accuracy. The method of the present invention is capable of positioning a nanostructure on the substrate within at least 20 nm of a predetermined position.

By "perovskites" it is meant to include $LaFO_3$, $SmFeO_3$ and

The present invention contemplates controlling the shape of the nanostructures by controlling the shape of the pattern in the mold or by the shape of the pattern in the sacrificial layer.

The present invention contemplates controlling the length of the nanostructures by controlling the length of the pattern in the mold or by the length of the pattern in the sacrificial layer.

The present invention contemplates controlling the position of the nanostructures by controlling the position of the pattern in the mold or by the position of the sacrificial layer.

Size reduction of nanostructures made in accordance with the present invention may be accomplished by producing a 20 nm (silicon, preferred) nanostructure and oxidize it at 800 °C for 20 minutes followed by HF dipping to remove the oxide. This treatment reduced the silicon dimension to ~ 12 nm, as shown in Fig 3(a). A high-resolution transmission electron microscopy (HRTEM) image also shows the single crystalline nature of the Si nanowire. Further oxidation at 800 °C for 10 minutes reduced the silicon dimension to ~ 7 nm, as shown in FIG 3(b). The

concave shape of the cross section of Si nanowire is due to lower oxidation rate for concave and convex surfaces (top and bottom) than planar surface (middle).

The nanostructures of the present invention are preferably doped. Doping of semiconductors is well known in the art, see for example Cui. et al. *J. Phys. Chem.* B **104**, 5213 (2000), Cui et al. *Science* **291**, 851 (2001) and Duan et al. *Nature* **409**, 66 (2001), the contents of which are hereby incorporated by reference in its entirety. Boron and phosphorus may be doped to provide p-type and n-type materials, respectively. Dopant concentration is controlled depending on the sensitivity desired of the resultant device. Techniques such as epitaxial overgrowth, diffusion, ion implantation are contemplated

Nanostructures have a large surface to volume ratio, which make its property sensitive to environmental perturbation on the surface. Especially, current flows through nanostructures within the proximity of the surface, electrical change due to the adsorption or desorption of molecules on the surface can influence the electron flow, which makes nanostructures good sensing devices.

The present invention contemplates that the nanoarrays made in accordance with the present invention are capable of use as chemical and biological sensors and catalytic devices. In one embodiment of the present invention contacts are attached to the nanostructures by standard lithographic techniques. The present invention contemplates that the in one embodiment the nanosensor described herein has a nanostructure that bridges the gap between two contacts through which electrical current may pass. Sections of the nanostructure may be suspended from the surface. Any changes in the properties of the nanostructure changes the electrical current and the measurement may indicate the presence of an analyte. The invention contemplates that the analyte may be in any phase, such as solution or gas. Arrays according to this invention are

capable of being constructed as a gate-less field effect transistor (FET) by functionalizing the nanostructure array with molecules, compositions or membranes capable of binding (ionically, covalently, van der walls or any other interaction, chemical or physical) with a target molecule of interest. The binding will then result in an increase or decrease in the carriers in the FET structure. Sensors constructed in accordance with the method of the present invention are capable of single molecule detection. Another advantage of sensors in accordance with the present invention is the possibility of dense arrays of nanostructures, which would further increase sensitivity.

A nanostructure device constructed according to the present invention may be made into a sensor device by functionalizing the surface of the nanostructure with a substance capable of responding in some way to the presence of a target molecule. The nanostructure array of the present invention is different from a typical FET because the surface is not covered by a metal gate, but is instead functionalized. When the target molecule contacts the functionalized surface of the nanowire a change in nanostructure electrical property (for example, conductance) or optical property occurs. The choice of functionalized substance/target molecule for use in accordance with this invention may be one well characterized in the art, for example the biotin-streptavidin ligand-receptor relationship. Other materials known in the art are also suitable as functionalized receptors or ligands for target molecules or analytes are calmodulin for sensing Ca^{2+} ions. Single stranded DNAs, antibodies, proteins are all contemplated as suitable for use as as functionalizing molecules. Other possibilities are any photoactive molecule, photonic nanoparticle, inorganic ion, inorganic nanoparticle, magnetic ion, magnetic nanoparticle, electronic nanoparticle, metallic nanoparticle, metal oxide nanoparticle, gold nanoparticle, gold-coated nanoparticle, carbon nanotube, nanocrystal, quantum dot, protein domain, enzyme,

hapten, antigen, biotin, digoxygenin, lectin, toxin, radioactive label, fluorophore, chromophore, or chemiluminescent molecule. It is contemplated that any molecule whose presence is a diagnostic of a particular human pathogenic organism, such as bacteria, protozoa, fungi, viruses and prions may be used.

The sensor may have a biologically and chemically protective coating that will inhibit non-specific interactions of non-targeted analytes. This may include a surfactant or lipid layer, a polymer layer or a micellar layer.

The invention also contemplates that a multitude of nanosensor arrays in accordance with the present invention may be functionalized with different organics and used to detect an array of molecules in parallel. Thus it is contemplated that one nanostructure is functionalized differently than another nanostructure. There may be 100, or 1000 or more nanostructures functionalized differently.

Inhibiting materials may cover the regions adjacent the nanostructures. The inhibiting material may be chosen depending on the desired use, but it must be impermeable to at lease one chemical, biochemical or biological target molecule. The inhibiting material layer may be impermeable to the target molecule, or semipermeable to the target molecule.

Electrical contacts to the sensor arrays may be made in accordance with those methods known in the art, such as electron-beam lithography , ion beam lithography, or photolithography. Suitable materials for the contacts include aluminum, titanium, titanium-tungsten, platinum, gold and copper.

The nanostructure sensor device may be configured to detect electrical signals before and after exposure to an analyte. Changes in signals can be related to detection of the analyte. Thus the sensor of the present invention may be coupled to a signal control and processing unit.

The drawings and figures used to describe the present invention are not necessarily to scale.

Examples

The following examples describe and illustrate aspects and features of specific implementations in accordance with the present invention. It should be understood the following is representative only, and that the invention is not limited by the detail set forth in these examples.

Example 1: Nanostructures/Nanostructure Arrays

The fabrication of one embodiment of the nanostructures/nanostructure arrays in accordance with the present invention is described below. Referencing FIG 1a and FIG 1b, a substrate (1) is provided. On top of which a sacrificial layer is deposited, (2). Via lithography, the sacrificial layer was patterned. A thin conformal layer (3) was then deposited on top of the patterned sacrificial layer. The conformal layer was anisotropically etched to expose the sacrificial layer. The sacrificial layer was then selectively removed. FIG 1a shows the conformal layer structure process as it was transferred into the substrate with further etching. This conformal layer structure was then removed leaving nanostructures/ nanostructure arrays of the same material as the substrate. The present invention contemplates the controlling of the height, width, length, shape, spacing, position, doping level, and/or composition of the nanostructures/ nanostructure arrays.

Example 2: Forming nanostructures in one embodiment of the present invention

Referencing FIG 2: Si(100) was used as the starting material, this is a preferred embodiment only, and not limiting. A 50 ~ 70 nm thermal oxide layer was grown on the Si wafers in a water

stream and oxygen at 850 °C. The optimal thickness of the thermal oxide was chosen from these two functional considerations. The layer should be thick enough to protect the substrate during the removal of the sacrificial polysilicon layer, while a thin layer is desired to minimize pattern broadening when forming the hard mask for subsequent silicon etching. A thin layer of polysilicon was deposited by low-pressure chemical vapor deposition using SiH_4 at 600 °C as the sacrificial layer. For improved mechanical stability, the layer thickness is 100 nm for generating Si features with sizes less than 30 nm and 400 nm for larger Si nanostructures. The polysilicon layer was then patterned by photolithography with a GCA 6200 wafer stepper, the resolution of which was around 600 nm. The pattern was transferred from the photoresist layer to the poly-silicon layer by plasma etching in a Lam Research 9400 TCP etcher. The conditions were 50 sccm Cl_2, 150 sccm HBr, pressure 15 mtorr, electrode temperature 50 °C, 300 W top electrode power and 150 W bottom electrode power with a bias of –160 V. This recipe etched poly-silicon with a speed of ~7 nm/s and produced a nearly vertical sidewall profile with an angle > 89.5°. It is also important to remove the polymers after the polysilicon etching. The estimated residue polymer thickness was 20 ~ 30 nm, which would significantly enlarge the nanometer pattern desired. The post etch step for the removal of the polymer was to dip the wafer in (100:1) HF for 10 s, strip the photoresist with oxygen plasma, followed by (100:1) HF 10 s then piranha [(4:1) H_2SO_4: H_2O_2] treated at 120 °C. Low temperature oxide (LTO) was deposited by low pressure chemical vapor deposition over the patterned polysilicon layer. The conditions were 5 sccm SiH_4 and 70 sccm O_2 at 450 °C. The deposition rate was ~ 3 nm/min. The step coverage is ~ 70% for thin films (<50 nm) and ~60% for thicker films, as shown in FIG 3(a) and 3(b), respectively. The thickness of the deposited LTO on the sidewall determines the minimum feature size. Anisotropic plasma etching was used to remove the LTO on the top of the sacrificial structure

and open the polysilicon structure (FIG 2f). The conditions were: 100 sccm CF_4, pressure 13 mtorr, 200 W top electrode power and 40 W bottom electrode power with a bias of –80 V. The etching speed was ~ 2 nm/s for LTO. This recipe also etches polysilicon and single crystal silicon with almost the same speed as for LTO. The polysilicon sacrificial layer was then removed with either wet etching or plasma etching (FIG 2g). Wet etching was conducted in $1:2_w$ KOH aqueous solution at 80 °C; the etching speed was around 17 nm/s for poly-silicon and 0.1 nm/s for LTO. Due to the etching non-uniformity, the complete removal of poly-silicon is generally not achieved until 2 minutes and this will severely undercuts the LTO spacer at 10 nm scale. Therefore, wet etching is not used for spacers smaller than 30 nm and plasma etching is used instead. The polysilicon plasma etching process is the same as the process for transferring pattern from photoresist into polysilicon layer and the etching selectivity of polysilicon to LTO is 22. The LTO pattern was then transferred to the thermal oxide layer by plasma etching with conditions 100 sccm CF_4, pressure 13 mtorr, 200 W top electrode power and 40 W bottom electrode power (FIG 2h). The resulting oxide pattern sidewall profile after this etching is not ideally vertical, showing some broadening for smaller spacers (< 30 nm, Fig 3(c)) and a noticeable undercut for larger spacers (> 50 nm, Fig 3(d)). The oxide pattern was transferred to silicon by plasma etching with conditions 50 sccm Cl_2, 150 sccm HBr, pressure 15 mtorr, electrode temperature 50 °C, 300 W top electrode power and 150 W bottom electrode power (FIG 2i). 20 nm silicon nanostructures can be routinely fabricated with this process, as shown in Fig 3(e) and Fig 3(f).

To reduce the silicon size further, the resulting 20 nm silicon nanostructure was oxidized at 800 °C for 20 minutes followed by HF dipping to remove the oxide. This treatment reduced the silicon dimension to ~ 12 nm, as shown in Fig 4(a). A high-resolution transmission electron

microscopy (HRTEM) image also shows the single crystalline nature of the Si nanostructure. Further oxidation at 800 °C for 10 minutes reduced the silicon dimension to ~ 7 nm, as shown in FIG 4(b). The concave shape of the cross section of Si nanostructure is due to lower oxidation rate for concave and convex surfaces (top and bottom) than planar surface (middle).

Example 3: Nanostructure fabrication by sidewall image transfer

Referring now to FIG 5a-5f where one embodiment in accordance with the present invention where fabricating a controlled nanostructure is illustrated. FIG 5a is a cross section view of the basic film stack. A nanoscale thin film 2 with desired chemical composition is formed on top of a substrate 1, which may comprise an insulating layer for electrical devices. A sacrificial layer 4 has been deposited on top of an optional protection layer 3. The substrate and nanoscale thin film are defined above, and the preferred embodiment is SOI wafer. The thickness of the nanoscale Si film can be reduced further by limited oxidation and removal of the oxidized portion of the film. The optional protection layer 3 prevents unintended damage or removal of the nanoscale film 2 and it can be formed by but not limited to either physical vapor deposition, chemical vapor deposition or direct growth by oxidation or nitrification of the film 3. The preferred material is silicon nitride or a silicon oxide, preferably silicon dioxide. The sacrificial layer 4 is a material that can be removed later by etching; the preferred material is polysilicon or a silicon oxide, preferably silicon dioxide. The sacrificial layer 4 can be patterned by standard lithography and etching, the pattern of which is shown in Fig 5b, which is a cross section view. Examples of lithography techniques suitable for this invention are photolithography, electron beam lithography, ion-beam lithography, etc, preferably photolithography. Etching is achieved either in a plasma environment (dry etching) or in a solution environment (wet etching), preferably dry etching. A conformal layer 5 is then deposited on the fabricated pattern, as in FIG

5c, followed by an anisotropic etch to remove all the conformal layer 5 except on the sidewall of sacrificial layer pattern 4, as depicted in FIG 5d. The conformal layer 5 should have a different etching characteristics than the sacrificial layer 4 so that either material can be selectively removed while remove very little of the other, such material pairs comprise, but not limited to polysilicon and silicon oxide, polysilicon and silicon nitride, silicon oxide and silicon nitride, photoresist and polysilicon, alumina gallium arsenate and gallium arsenate, etc. The preferred material pair is polysilicon and a silicon oxide, preferably silicon dioxide.

Once the sacrificial layer 4 is exposed, it can be selectively removed by either dry or wet etching. FIG 5E shows the remaining conformal layer structure 5 has approximately equal width to the film thickness, which can be less than 50nm. This sublithographic images then can be transferred through the protective layer 3 into the desired nanoscale film layer 2 by etching or ion milling, as shown in FIG 5f. After removal of the protective layer 3, nanostructures with any desired chemical composition are fabricated in layer 2, as shown in FIG 5g.

The present invention contemplates that the width of the nanostructure can be further reduced by either controlled etching or converting to a material that can be selectively removed. In one embodiment of the present invention, polymer nanostructures can be further reduced in size by controlled etching in oxygen plasma. In another embodiment of the present invention, Si nanostructures can be further reduced in size by thermal oxidation to convert to SiO_2, which then can be removed by HF etching. In another embodiment of the present invention, Si nanostructures can be further reduced in size by controlled XeF_2 etch.

Example 4: Controlling the position, length and shape of nanostructure

The position, length and shape of the nanostructures may be predetermined by the initial pattern in the sacrificial layer 4 (FIG 5), but can also be modified after fabrication. FIG 6a is an

example of a 3-D view of two different shapes of patterns created in the sacrificial layer 4, one is a rectangle, the other is a circle. The shapes are determined by standard lithography, and these specific shapes provided are intended as examples, not as limitations. FIG 6b shows the shape and position of the nanostructures 2 created on the substrate 1. The shape of the nanostructure follows the boundary of the sacrificial layer pattern 4, and the position of the nanostructure is determined by the position of the sacrificial layer pattern 4.

Since the position of the nanostructure can be pre-determined, standard lithography methods, preferably photolithography, can be applied to change the length and/or shape of the nanostructure by masking the desired part with resist 6 and removing the exposed part with etching techniques, as illustrated in FIG 6c. In one embodiment contemplated by the present invention, one can mask half of the structure off and remove the other half. This will result in the fabrication of half circle and half of the rectangle on the substrate 1, shown in FIG 6d. Accordingly any complex shape can be accomplished.

The present invention contemplates the formation of an open ended structure as in FIG 6d, a closed ended structure as in FIG 6b, or both.

Following the teaching of the method, one can readily appreciate that the present invention contemplates controlling the composition of the nanostructures by forming a thin film of desired composition on a substrate. Further, the present invention contemplates controlling the height of the nanostructures by either timed etching into the desired film or the thickness of the desired film. The preferred method is by controlling the thickness of the desired film. The present invention contemplates controlling the width of the nanostructures by either controlling the thickness of the conformal layer or the procedures of after fabrication modification.

The present invention contemplates further modification of shape and length of the nanostructure after fabrication with standard lithography method to remove unwanted parts.

Example 5: Nanostructure fabrication by combining sidewall image transfer with imprint lithography

Referring now to FIG 7 and 8, where other embodiments in accordance with the present invention whereby a method of fabricating controlled nanostructure is illustrated. FIG 7a is a cross section view of the basic film stack. A sacrificial layer 9 has been deposited on top of an optional protection layer 8 on a substrate 7. The substrate is defined above, and the preferred embodiment is Si wafer. The optional protection layer 8 prevents unintended damage or removal of the substrate 7 and it can be formed by but not limited to either physical vapor deposition, chemical vapor deposition or direct growth by oxidation or nitrification of the substrate 7. The preferred material is silicon nitride or silicon oxide. The sacrificial layer 9 is a material that can be removed later by etching; the preferred material is polysilicon or a silicon oxide, preferably silicon dioxide. The sacrificial layer 9 can be patterned by standard lithography and etching, the pattern of which is shown in FIG 7b. Examples of standard lithography are photolithography, electron beam lithography, ion-beam lithography, etc, preferably photolithography. Etching is achieved either in a plasma environment (dry etching) or in a solution environment (wet etching), preferably dry etching. A conformal layer 10 is then deposited on the fabricated pattern, as in FIG 7c, followed by an anisotropic etch to remove all the conformal layer 10 except on the sidewall of sacrificial layer pattern 9, as depicted in FIG 7d. The conformal layer 10 should have a different etching characteristics than the sacrificial layer 9 so that either material can be selectively removed while remove very little of the other, such material pairs comprise, but not limited to polysilicon and a silicon oxide, preferably silicon dioxide, polysilicon and silicon

nitride, a silicon oxide, preferably silicon dioxide and silicon nitride, photoresist and polysilicon, alumina gallium arsenate and gallium arsenate, etc. The preferred material pair is polysilicon and a silicon oxide, preferably silicon dioxide.

Once the sacrificial layer 9 is exposed, it can be selectively removed by either dry or wet etching. FIG 7e shows the remaining conformal layer structure 10 has approximately equal width to the film thickness, which can be less than 50nm. This sublithographic images then can be transferred through the protective layer 8 into substrate 7 by etching or ion milling, as shown in FIG 7f. After removing of protective layer 8, nanostructures with desired chemical composition are fabricated in substrate 7.

The width of the nanostructure can be further reduced by either controlled etching or converting to a material that can be selectively removed. In one embodiment of the present invention, Si nanostructures can be further reduced in size by controlled XeF_2 etch. In one embodiment of the present invention, Si nanostructures can be further reduced in size by thermal oxidation to convert to SiO_2, which then can be removed by HF etching.

The position, length and shape of the nanostructures are determined by the initial pattern in the sacrificial layer 9, but can also be modified after fabrication, similar to the teaching related to FIG 6. The nanostructures thus fabricated on the substrate 7 can be used as a mold to transfer the nanostructure pattern.

Example 6: Transfer of a nanostructure pattern

FIGs 8a – 8e illustrate the process of imprint lithography to transfer the pattern onto a substrate. FIG 8a is a cross section view of a mold thus fabricated by the above method pressed against a substrate 12 coated with a resist 11. A thickness variation is created in the resist layer 11. Upon separation, an anisotropic etching process is used to transfer the pattern into entire

resist, as shown in FIG 8b. The desired composition of materials or layers of materials then can be deposited vertically onto the patterned substrate 12, preferably by evaporation or sputtering in vacuum environment, as shown in FIG 8c. In the next step, the resist 11 is removed by dissolution in solvent, which left the deposited material 13 on the substrate 12, as shown in FIG 8d. The deposited material 13 can also act as a mask to further transfer the nanostructure pattern into substrate 12, as depicted in FIG 8e. The present invention contemplates controlling the shape of the nanostructures by controlling the shape of the pattern in the mold, which is further controlled in the mold fabrication process by the shape of the pattern in the sacrificial layer.

The present invention contemplates controlling the length of the nanostructures by controlling the length of the pattern in the mold, which is further controlled in the mold fabrication process by the length of the pattern in the sacrificial layer.

The present invention contemplates controlling the position of the nanostructures by controlling the position of the pattern in the mold, which is further controlled in the mold fabrication process by the position of the sacrificial layer.

Example 8: Nanostructure sensing devices

Shown in FIG 9a-9g are examples of methods for the fabrication of nanoscale sensing devices by sidewall image transfer method. Referencing FIG 9a-9g, (15) is the nanoscale thick semiconductor layer; (16) is a protective layer; (17) is a thin conformal layer; (18) is a resist; (19) is a contact. FIG 9g shows an embodiment where the nanostructure is functionalized with a functionalizing agent, R.

FIG 10a shows one embodiment of an array in accordance with the present invention. FIG 10b shows a sensor device in accordance with one embodiment of the invention. (23) is an

insulator layer; (24) is a nanostructure sensing element comprising TiO_2, SiO_2, or the like and (25) is a contact or conductor.

Example 7: Nanostructure/Nanostructure Array Sensors: Nanostructures/Nanostructure Arrays and Contacts Fabricated in Parallel (at the same time)

The invention contemplates that nanostructure arrays and sensors made using the nanoarrays have contacts that are effectively in intimate contact and contiguous with the top semiconductor layer of the substrate, for example see FIG 9d, (15). In this embodiment the top substrate layer, the contact and the nanostructure would all be of the same semiconductor material, preferably Si. Nanostructure array sensors in accordance with the present invention and possession the positional and compositional control may be fabricated in the following manner, with reference to FIG 11. On top of a substrate (in this embodiment, the substrate (1) comprises a multilayer structure of a semiconductor/insulator/semiconductor), an insulating layer (2) may be deposited. A sacrificial layer (3) may then be deposited on top of this insulating layer. A photoresist (5) may be spin-cast on top of the sacrificial layer, and a pattern will be generated in the photoresist via photolithography. The photoresist will serve as a mask to pattern the sacrificial layer through etching. Preferably the etch process is stopped at the insulating layer. The photoresist is then removed. A conformal layer (4) may be deposited over the patterned sacrificial layer. Referencing FIG 12, the top of the conformal layer (4) may be removed by etching, thus exposing the top of the sacrificial layer pattern, (3). The sacrificial layer pattern will be selectively removed via etching, leaving conformal layer nanostructures, (8). The conformal layer nanostructures will serve as a mask to etch into the top layer of the substrate. It is noted that after this step, FIG 12 now omits the insulator layer 2. The conformal layer nanostructures will then be removed via etching, leaving behind nanostructures of the substrate

material. Referencing FIG 13, there is described another series of photolithography steps to fabricate photoresist structures (5) on top of portions of the substrate material nanostructures. The exposed substrate material nanostructures will be etched away, followed by removal of the photoresist via etching. This creates a nanostructure having a shape of a half circle. This nanostructure is the top layer of the substrate that was started with. The nanostructure is made from the original top layer and everything but the nanostructure has been etched away.

Example 8: Forming a sensor and functionalization

Referencing FIG 14, substrate is (1) which comprises a lower layer that may comprise a semiconductor, shown, but other materials are contemplated, an intemediate layer comprising an insulator and a top layer comprising a nanostructure, formed as in Example 7. The nanostructure is fitted with contacts by typical lithograpic techniques and functionalized. Nanostructures are created such that depending on the desired species detection, the surface of the substrate material nanostructures will be functionalized with the appropriate material.

Example 9: Nanostructure/Nanostructure Array Sensors: Nanostructures/Nanostructure Arrays and Contacts Fabricated in Series (at the same time)

The present invention contemplates that nanostructure arrays and sensors made using the arrays have contacts that effectively are positioned on top of the nanostructure, for example see FIG 5f, (19). In this embodiment it is preferred that the top of the substrate be Si and the nanostructure and contact are of a different material. These nanostructure/nanostructure array sensors may be fabricated in the following manner. Conformal layer nanostructures are produced as recited in Example 7. These structures would be on top of the insulating layer (2), and are (4) in FIG 15. Referencing FIG 16, another series of photolithography steps may be performed to leave behind photoresist structures on top of portions of the conformal layer

nanostructures. The photoresist structures and the conformal layer nanostructures will serve as masks to etch into the substrate. The photoresist and conformal layer nanostructures will then be removed via etching. This will produce substrate material nanostructures and substrate material contacts. Ion implantation will be utilized to create high doping areas for the contacts and low doping areas (the nanostructures) for the detection area. This enables the electron flow control between contacts. Depending on the desired species detection, the surface of the substrate material nanostructures will be functionalized with the appropriate material, FIG 17.

Example 10: Nanoimprint Lithography for Nanostructure/Nanostructure Array Pattern Transfer

In one embodiment of the present invention there is contemplated a nanostructure/nanostructure array pattern made by transferring to a different material via imprint lithography. The material chosen may vary depending on the intended use. First, the nanostructure/nanostructure array pattern may be generated as described in any of the above embodiments. This is intended to be used as the mold, FIG 18 and 19 (1: mold/mold material; 2:substrate; 3: imprint resist; 4: desired material depending on application). A new second substrate was then selected. An imprint resist was spin-casted onto the substrate is the imprint resist. The mold was then pressed into the resist layer of the second substrate at the necessary temperature and pressure. The mold was then separated from the resist layer. The residual resist of the second substrate was etched away to expose the substrate. The desired material was then deposited onto this second substrate, followed by lift-off of the imprint resist.

Example 11: Fabrication of a suspended nanostructure

A nanostructure may be created as described in Example 3, FIG 5. The underlying optional insulator layer in the substrate or the substrate can be selectively removed by wet or dry etching at intended, predetermined positions or locations to create suspended nanostructures.

Suspended Si nanostructures can be created by incorporating a SiO_2 layer in the substrate at the start of the fabrication process and removing the underlying SiO_2 layer at desired locations in solutions containing fluorinated agent after the Si nanostructure is fabricated by process shown in Example 3. The rest of the locations where SiO_2 is intended to keep are masked by lithography method, preferably photolithography. FIG 20b shows an embodiment where the nanostructure is "suspended". By patterning FIG 20a with lithography and exposisng the area where SiO_2 is to be removed, and exposing the unmasked SiO_2 to HF to disolive it, and removing the resist, the suspended nanostructure may be fabricated.

Although the foregoing invention has been described in some detail for purposes of clarity of understanding, those skilled in the art will appreciate that various adaptations and modifications of the just described preferred embodiments can be configured without departing from the scope and spirit of the invention. Moreover, the described processing distribution and classification engine features of the present invention may be implemented together or independently. Therefore, the described embodiments should be taken as illustrative and not restrictive, and the invention should not be limited to the details given herein but should be defined by the following claims and their full scope of equivalents.

CLAIMS

What is claimed is:

1. A method of fabricating a nanostructure array comprising:

providing a substrate having a top layer, and

depositing a sacrificial layer having a first etching characteristic,

patterning the sacrificial layer,

forming a thin conformal layer having a second etching characteristic over the patterned sacrificial structure,

wherein the first and second etching characteristics are different,

anisotropically etching the conformal layer to create a pattern,

removing the sacrificial layer,

transferring the resulting conformal layer structure to the substrate by etching, and

removing any remaining conformal layer structure,

thereby creating at least one nanostructure in the top layer.

2. The method of fabricating a nanostructure array of claim 1, further comprising:

reducing the dimension of the nanostructure.

3. The method of fabricating a nanostructure array of claim 2, wherein:

the reduction in dimension is accomplished by controlled etching or converting to a material that has different etching characteristics and removing the material.

4. The method of fabricating a nanostructure array of claim 3, wherein:

the nanostructure comprises Si, and

the reduction in dimension is accomplished by thermal oxidation to convert to SiO_2, and

contacting with an etchant to remove the oxide.

5. The method of fabricating a nanostructure array of claim 3, wherein:

the nanostructure comprises Si,

and the reduction in dimension is accomplished by controlled XeF_2 etch.

6. The method of fabricating a nanostructure array of claim 1, wherein:

the shape of at least one nanostructure is modified.

7. The method of fabricating a nanostructure array of claim 6, wherein:

at least part of the nanostructure is masked with resist, and

any unmasked part is removed by etching.

8. The method of fabricating a nanostructure array of claim 7, wherein:

the resist is photoresist,

and is patterned by photolithography.

9. The method of fabricating a nanostructure array of claim 7, wherein:

the resist is electron beam resist or ion beam resist,

and is patterned by electron beam lithography or ion beam lithography.

10. The method of fabricating a nanostructure array of claim 1, wherein:

the substrate is a multilayer structure, comprising:

a lower layer comprising silicon,

an intermediate layer comprising an insulating material,

an upper layer comprising a mateial chosen from the group consisting of semiconductors, metals and oxides, all of which may be doped or undoped.

11. The method of fabricating a nanostructure array of claim 10, wherein:

the insulating material is chosen from the group consisting of nitrides, oxides and polymers.

12. The method of fabricating a nanostructure array of claim 10, wherein:

the semiconductor is selected from the group consisting of group IV, III-V, II-VII semiconductors and semiconducting oxides, and it may be doped or undoped.

13. The method of fabricating a nanostructure array of claim 1, further comprising:

providing a protective layer below the sacrificial layer.

14. The method of fabricating a nanostructure array of claim 1, wherein:

patterning the sacrificial layer is done by photolithography, electron beam lithography or ion beam lithography.

15. The method of fabricating a nanostructure array of claim 1, wherein:

the conformal layer comprises silicon oxide, silicon nitride and polysilicon.

16. The method of fabricating a nanostructure array of claim 1, wherein:

the conformal layer can be formed by chemical vapor deposition, spin coating, sputtering, evaporation or chemical reaction with the sacrificial layer.

17. The method of fabricating a nanostructure array of claim 1, wherein:

the sacrificial layer is removed by either plasma or wet etching.

18. The method of fabricating a nanostructure array of claim 1, further comprising:

forming a contact in intimate contact with at least one nanostructure.

19. The method of fabricating a nanostructure array of claim 18, wherein:

the contact is formed by lithography.

20. The method of fabricating a nanostructure array of claim 19, wherein:

the lithography is photolithography.

21. The method of fabricating a nanostructure array of claim 18, wherein:

the contact is formed by forming a conducting film,

masking the contact area by lithography, and

ething any exposed film away.

22. The method of fabricating a nanostructure array of claim 1, wherein:

the substrate and the top layer comprise the same material, and

are separated by an insulator layer.

23. The method of fabricating a nanostructure array of claim 1, wherein:

the top layer comprises Si.

24. The method of fabricating a nanostructure array of claim 1, wherein:

at least one nanostructure is fabricated on a predetermined location with positional control.

25. The method of fabricating a nanostructure array of claim 1, wherein:

there are between 1000 and 1 billion nanostructures on the array, and

are fabricated on a predetermined location and with positional control.

26. The method of fabricating a nanostructure array of claim 1, further comprising:

functionalizing at least one nanostructure with a functionalizing agent.

27. The method of fabricating a nanostructure array of claim 1, further comprising:

functionalizing more than one nanostructure with a functionalizing agent.

28. The method of fabricating a nanostructure array of claim 27, wherein:

the functionalizing agent is not the same for each nanostucture.

29. The method of fabricating a nanostructure array of claim 27, wherein more than one nanostructure is functionalized with one or more receptors selected from the group consisting of ss-DNAs, proteins, antibodies, platinum, photoactive molecules, photonic nanoparticle, inorganic ion, inorganic nanoparticle, magnetic ion, magnetic nanoparticle, electronic nanoparticle, metallic nanoparticle, metal oxide nanoparticle, gold nanoparticle, gold-coated nanoparticle, carbon nanotube, nanocrystal, quantum dot, protein domain, enzyme, hapten, antigen, biotin, digoxygenin, lectin, toxin, radioactive label, fluorophore, chromophore, or a chemiluminescent molecule.

30. The method of fabricating a nanostructure array of claim 1, wherein:

the nanostructure comprises the top layer of the substrate.

31. The method of fabricating a nanostructure array of claim 1, further comprising:

at least one contact positioned on a top layer of the substrate, and

the contact, the nanostructure and the top layer comprise the same material.

32. The method of fabricating a nanostructure array of claim 31, wherein:

there are a plurality of nanostructures, and

at least one contact is positioned in intimate contact with more than one nanostructure.

33. The method of fabricating a nanostructure array of claim 1, wherein:

the nanostructure comprises a material selected from the group consisting of SnO_2, TiO_2, Fe oxides, ZnO, WO_3, Ga_2O_3 and perovskites.

34. A method of fabricating a nanostructure array comprising at least one nanostructure positioned in a predetermined location, said method comprising:

providing a substrate having a sacrificial layer having a first etching characteristic,

patterning the sacrificial layer.

35. The method of fabricating a nanostructure array of claim 34, further comprising:

reducing the dimension of the nanostructure.

36. The method of fabricating a nanostructure array of claim 35, wherein:

the reduction in dimension is accomplished by controlled etching or converting to a material that has different etching characteristics and removing the material.

37. The method of fabricating a nanostructure array of claim 36, wherein:

the nanostructure comprises Si, and

the reduction in dimension is accomplished by thermal oxidation to convert to SiO_2, and

contacting with an etchant to remove the oxide.

38. The method of fabricating a nanostructure array of claim 36, wherein:

the nanostructure comprises Si,

and the reduction in dimension is accomplished by controlled XeF_2 etch.

39. The method of fabricating a nanostructure array of claim 34, wherein:

the shape of at least one nanostructure is modified.

40. The method of fabricating a nanostructure array of claim 39, wherein:

at least part of the nanostructure is masked with resist, and

any unmasked part is removed by etching.

41. The method of fabricating a nanostructure array of claim 40, wherein:

the resist is photoresist,

and is patterned by photolithography.

42. The method of fabricating a nanostructure array of claim 40, wherein:

the resist is electron beam resist or ion beam resist,

and is patterned by electron beam lithography or ion beam lithography.

43. The method of fabricating a nanostructure array of claim 34, wherein:

the substrate is a multilayer structure, comprising:

a lower layer comprising silicon,

an intermediate layer comprising an insulating material,

an upper layer comprising a mateial chosen from the group consisting of semiconductors, metals and oxides, all of which may be doped or undoped.

44. The method of fabricating a nanostructure array of claim 43, wherein:

the insulating material is chosen from the group consisting of nitrides, oxides and polymers.

45. The method of fabricating a nanostructure array of claim 43, wherein:

the semiconductor is selected from the group consisting of group IV, III-V, II-VII semiconductors and semiconducting oxides, and it may be doped or undoped.

46. The method of fabricating a nanostructure array of claim 34, further comprising:

providing a protective layer below the sacrificial layer.

47. The method of fabricating a nanostructure array of claim 34, wherein:

patterning the sacrificial layer is done by photolithography, electron beam lithography or ion beam lithography.

48. The method of fabricating a nanostructure array of claim 34, wherein:

the is a conformal layer, and

the conformal layer comprises silicon oxide, silicon nitride and polysilicon.

49. The method of fabricating a nanostructure array of claim 48, wherein:

the conformal layer can be formed by chemical vapor deposition, spin coating, sputtering, evaporation or chemical reaction with the sacrificial layer.

50. The method of fabricating a nanostructure array of claim 1, wherein:

the sacrificial layer is removed by either plasma or wet etching.

51. The method of fabricating a nanostructure array of claim 34, further comprising:

forming a contact in intimate contact with at least one nanostructure.

52. The method of fabricating a nanostructure array of claim 51, wherein:

the contact is formed by lithography.

53. The method of fabricating a nanostructure array of claim 52, wherein:

the lithography is photolithography.

54. The method of fabricating a nanostructure array of claim 51, wherein:

the contact is formed by forming a conducting film,

masking the contact area by lithography, and

ething any exposed film away.

55. The method of fabricating a nanostructure array of claim 34, wherein:

the substrate and the top layer comprise the same material, and

are separated by an insulator layer.

56. The method of fabricating a nanostructure array of claim 34, wherein:

the top layer comprises Si.

57. The method of fabricating a nanostructure array of claim 34, wherein:

at least one nanostructure is fabricated on a predetermined location with positional control.

58. The method of fabricating a nanostructure array of claim 34, wherein:

there are between 1000 and 1 billion nanostructures on the array, and are fabricated on a predetermined location and with positional control.

59. The method of fabricating a nanostructure array of claim 34, further comprising:

functionalizing at least one nanostructure with a functionalizing agent.

60. The method of fabricating a nanostructure array of claim 34, further comprising:

functionalizing more than one nanostructure with a functionalizing agent.

61. The method of fabricating a nanostructure array of claim 60, wherein:

the functionalizing agent is not the same for each nanostucture.

62. The method of fabricating a nanostructure array of claim 60, wherein more than one nanostructure is functionalized with one or more receptors selected from the group consisting of ss-DNAs, proteins, antibodies, platinum, photoactive molecules, photonic nanoparticle, inorganic ion, inorganic nanoparticle, magnetic ion, magnetic nanoparticle, electronic nanoparticle, metallic nanoparticle, metal oxide nanoparticle, gold nanoparticle, gold-coated nanoparticle, carbon nanotube, nanocrystal, quantum dot, protein domain, enzyme, hapten, antigen, biotin, digoxygenin, lectin, toxin, radioactive label, fluorophore, chromophore, or a chemiluminescent molecule.

63. The method of fabricating a nanostructure array of claim 34, wherein:

the nanostructure comprises the top layer of the substrate.

64. The method of fabricating a nanostructure array of claim 34, further comprising:

at least one contact positioned on a top layer of the substrate, and

the contact, the nanostructure and the top layer comprise the same material.

65. The method of fabricating a nanostructure array of claim 34, wherein:

there are a plurality of nanostructures, and

at least one contact is positioned in intimate contact with more than one nanostructure.

66. The method of fabricating a nanostructure array of claim 34, wherein:

the nanostructure comprises a material selected from the group consisting of SnO_2, TiO_2, Fe oxides, ZnO, WO_3, Ga_2O_3 and perovskites.

67. A method of fabricating a nanostructure array, comprising

providing a first substrate,

depositing a sacrificial layer having a first etching characteristic,

patterning the sacrificial layer,

depositing a thin conformal layer having a second etching characteristic o over the patterned sacrificial structure, wherein

the first and second etching characteristics are different,

anisotropically etching the conformal layer to create a pattern,

removing the sacrificial layer,

transferring the resulting conformal layer structure to the first substrate by etching, and

removing any remaining conformal layer structure, thus creating nanostructure array pattern on the first substrate,

contacting the nanostructure array pattern with a second substrate containing a resist to create an impression pattern in the resist,

anisotropically transferring the pattern into entire resist, and

vertically depositing a desired composition onto the pattern and removing the resist,

thereby creating at least one nanostructure on the second substrate.

68. The method of fabricating a nanostructure array of claim 67, further comprising:

reducing the dimension of the nanostructure.

69. The method of fabricating a nanostructure array of claim 68, wherein:

the reduction in dimension is accomplished by controlled etching or converting to a material that has different etching characteristics and removing the material.

70. The method of fabricating a nanostructure array of claim 69, wherein:

the nanostructure comprises Si, and

the reduction in dimension is accomplished by thermal oxidation to convert to SiO_2, and

contacting with an etchant to remove the oxide.

71. The method of fabricating a nanostructure array of claim 69, wherein:

the nanostructure comprises Si,

and the reduction in dimension is accomplished by controlled XeF_2 etch.

72. The method of fabricating a nanostructure array of claim 67, wherein:

the shape of at least one nanostructure is modified.

73. The method of fabricating a nanostructure array of claim 72, wherein:

at least part of the nanostructure is masked with resist, and

any unmasked part is removed by etching.

74. The method of fabricating a nanostructure array of claim 73, wherein:

the resist is photoresist,

and is patterned by photolithography.

75. The method of fabricating a nanostructure array of claim 73, wherein:

the resist is electron beam resist or ion beam resist,

and is patterned by electron beam lithography or ion beam lithography.

76. The method of fabricating a nanostructure array of claim 67, wherein:

the substrate is a multilayer structure, comprising:

a lower layer comprising silicon,

an intermediate layer comprising an insulating material,

an upper layer comprising a mateial chosen from the group consisting of semiconductors, metals and oxides, all of which may be doped or undoped.

77. The method of fabricating a nanostructure array of claim 76, wherein:

the insulating material is chosen from the group consisting of nitrides, oxides and polymers.

78. The method of fabricating a nanostructure array of claim 76, wherein:

the semiconductor is selected from the group consisting of group IV, III-V, II-VII semiconductors and semiconducting oxides, and it may be doped or undoped.

79. The method of fabricating a nanostructure array of claim 67, further comprising:

providing a protective layer below the sacrificial layer.

80. The method of fabricating a nanostructure array of claim 67, wherein:

patterning the sacrificial layer is done by photolithography, electron beam lithography or ion beam lithography.

81. The method of fabricating a nanostructure array of claim 67, wherein:

the conformal layer comprises silicon oxide, silicon nitride and polysilicon.

82. The method of fabricating a nanostructure array of claim 67, wherein:

the conformal layer can be formed by chemical vapor deposition, spin coating, sputtering, evaporation or chemical reaction with the sacrificial layer.

83. The method of fabricating a nanostructure array of claim 67, wherein:

the sacrificial layer is removed by either plasma or wet etching.

84. The method of fabricating a nanostructure array of claim 67, further comprising:

forming a contact in intimate contact with at least one nanostructure.

85. The method of fabricating a nanostructure array of claim 84, wherein:

the contact is formed by lithography.

86. The method of fabricating a nanostructure array of claim 85, wherein:

the lithography is photolithography.

87. The method of fabricating a nanostructure array of claim 84, wherein:

the contact is formed by forming a conducting film,

masking the contact area by lithography, and

ething any exposed film away.

88. The method of fabricating a nanostructure array of claim 67, wherein:

the substrate and the top layer comprise the same material, and

are separated by an insulator layer.

89. The method of fabricating a nanostructure array of claim 67, wherein:

the top layer comprises Si.

90. The method of fabricating a nanostructure array of claim 67, wherein:

at least one nanostructure is fabricated on a predetermined location with positional control.

91. The method of fabricating a nanostructure array of claim 67, wherein:

there are between 1000 and 1 billion nanostructures on the array, and

are fabricated on a predetermined location and with positional control.

92. The method of fabricating a nanostructure array of claim 67, further comprising:

functionalizing at least one nanostructure with a functionalizing agent.

93. The method of fabricating a nanostructure array of claim 67, further comprising:

functionalizing more than one nanostructure with a functionalizing agent.

94. The method of fabricating a nanostructure array of claim 38, wherein:

the functionalizing agent is not the same for each nanostucture.

95. The method of fabricating a nanostructure array of claim 67, wherein more than one nanostructure is functionalized with one or more receptors selected from the group consisting of ss-DNAs, proteins, antibodies, platinum, photoactive molecules, photonic nanoparticle, inorganic ion, inorganic nanoparticle, magnetic ion, magnetic nanoparticle, electronic nanoparticle, metallic nanoparticle, metal oxide nanoparticle, gold nanoparticle, gold-coated nanoparticle, carbon nanotube, nanocrystal, quantum dot, protein domain, enzyme, hapten, antigen, biotin, digoxygenin, lectin, toxin, radioactive label, fluorophore, chromophore, or a chemiluminescent molecule.

96. The method of fabricating a nanostructure array of claim 67, wherein:

the nanostructure comprises the top layer of the substrate.

97. The method of fabricating a nanostructure array of claim 67, further comprising:

at least one contact positioned on a top layer of the substrate, and

the contact, the nanostructure and the top layer comprise the same material.

98. The method of fabricating a nanostructure array of claim 67, wherein:

there are a plurality of nanostructures, and

at least one contact is positioned in intimate contact with more than one nanostructure.

99. The method of fabricating a nanostructure array of claim 67, wherein:

the nanostructure comprises a material selected from the group consisting of SnO_2, TiO_2, Fe oxides, ZnO, WO_3, Ga_2O_3 and perovskites.

100. A sensor device, comprising:

a substrate,

an insulating layer, and

at least one nanostructure overlying the insulating layer in a predetermined position.

101. The sensor device of claim 100, further comprising:

at least one nanostructure is functionalized with a receptor selected from the group consisting of ss-DNAs, proteins, antibodies, platinum, photoactive molecules, photonic nanoparticle, inorganic ion, inorganic nanoparticle, magnetic ion, magnetic nanoparticle, electronic nanoparticle, metallic nanoparticle, metal oxide nanoparticle, gold nanoparticle, gold-coated nanoparticle, carbon nanotube, nanocrystal, quantum dot, protein domain, enzyme, hapten, antigen, biotin, digoxygenin, lectin, toxin, radioactive label, fluorophore, chromophore, or chemiluminescent molecule.

102. The sensor device of claim 100, wherein:

the substrate comprises silicon.

103. The sensor device of claim 100, wherein:

at least one nanostructure is suspended from the substrate.

104. The sensor device of claim 100, wherein:

the nanostructure has a shape comprising open ended and/or closed ended.

105. The sensor device of claim 100, wherein:

the substrate is a multilayer structure, comprising:

a lower layer comprising silicon,

an intermediate layer comprising an insulating material,

an upper layer comprising a mateial chosen from the group consisting of semiconductors, metals and oxides, all of which may be doped or undoped.

106. The sensor device of claim 105, wherein:

the insulating material is chosen from the group consisting of nitrides, oxides and polymers.

107. The sensor device of claim 106, wherein:

the semiconductor is selected from the group consisting of group IV, III-V, II-VII semiconductors and semiconducting oxides, and it may be doped or undoped.

108. The sensor device of claim 100, wherein:

the substrate comprises a top layer, and

the substrate and the top layer comprise the same material, and

are separated by an insulator layer.

109. The sensor device of claim 108, wherein:

the top layer comprises Si.

110. The sensor device of claim 100, wherein:

there are between 1000 and 1 billion nanostructures on the array.

111. The sensor device of claim 100, wherein:

the nanostructure is functionalized with at least one functionalizing agent

112. The sensor device of claim 100, wherein:

there are a plurality of nanostructures and more than one nanostructure is functionalized with at least one functionalizing agent.

113. The sensor device of claim 112, wherein:

the functionalizing agent is not the same for each nanostructure.

114. The sensor device of claim 100, wherein:

the nanostructure comprises a top layer of the substrate.

115. The sensor device of claim 100, further comprising:

at least one contact positioned on a top layer of the substrate, and

the contact, the nanostructure and the top layer comprise the same material.

116. The sensor device of claim 100, wherein:

there are a plurality of nanostructures, and

at least one contact is positioned in intimate contact with more than one nanostructure.

117. The sensor device of claim 100, wherein:

the nanostructure comprises a material selected from the group consisting of SnO_2, TiO_2, Fe oxides, ZnO, WO_3, Ga_2O_3 and perovskites.

118. A nanostructure array, comprising:

a substrate,

an insulating layer, and

at least one nanostructure overlying the insulating layer in a predetermined position.

119. The nanostructure array of claim 118, further comprising:

at least one nanostructure is functionalized with a receptor selected from the group consisting of ss-DNAs, proteins, antibodies, platinum, photoactive molecules, photonic nanoparticle, inorganic ion, inorganic nanoparticle, magnetic ion, magnetic nanoparticle, electronic nanoparticle, metallic nanoparticle, metal oxide nanoparticle, gold nanoparticle, gold-coated nanoparticle, carbon nanotube, nanocrystal, quantum dot, protein domain, enzyme, hapten, antigen, biotin, digoxygenin, lectin, toxin, radioactive label, fluorophore, chromophore, or chemiluminescent molecule.

120. The nanostructure array of claim 118, wherein:

the substrate comprises silicon.

121. The nanostructure array of claim 118, wherein:

at least one nanostructure is suspended from the substrate.

122. The nanostructure array of claim 118, wherein:

the nanostructure has a shape comprising open ended and/or closed ended.

123. The nanostructure array of claim 118, wherein:

the substrate is a multilayer structure, comprising:

a lower layer comprising silicon,

an intermediate layer comprising an insulating material,

an upper layer comprising a mateial chosen from the group consisting of semiconductors, metals and oxides, all of which may be doped or undoped.

124. The nanostructure array of claim 118, wherein:

the insulating material is chosen from the group consisting of nitrides, oxides and polymers.

125. The nanostructure array of claim 123, wherein:

the semiconductor is selected from the group consisting of group IV, III-V, II-VII semiconductors and semiconducting oxides, and it may be doped or undoped.

126. The nanostructure array of claim 118, wherein:

the substrate comprises a top layer, and

the substrate and the top layer comprise the same material, and

are separated by an insulator layer.

127. The nanostructure array of claim 126, wherein:

the top layer comprises Si.

128. The nanostructure array of claim 118, wherein:

there are between 1000 and 1 billion nanostructures on the array.

129. The nanostructure array of claim 118, wherein:

the nanostructure is functionalized with at least one functionalizing agent

130. The nanostructure array of claim 118, wherein:

there are a plurality of nanostructures and more than one nanostructure is functionalized with at least one functionalizing agent.

131. The nanostructure array of claim 130, wherein:

the functionalizing agent is not the same for each nanostructure.

132. The nanostructure array of claim 118, wherein:

the nanostructure comprises a top layer of the substrate.

133. The nanostructure array of claim 118, further comprising:

at least one contact positioned on a top layer of the substrate, and

the contact, the nanostructure and the top layer comprise the same material.

134. The nanostructure array of claim 118, wherein:

there are a plurality of nanostructures, and

at least one contact is positioned in intimate contact with more than one nanostructure.

135. The nanostructure array of claim 118, wherein:

the nanostructure comprises a material selected from the group consisting of SnO_2, TiO_2, Fe oxides, ZnO, WO_3, Ga_2O_3 and perovskites.

ABSTRACT OF THE DISCLOSURE

Fabrication methods disclosed herein provide for a nanoscale structure or a pattern comprising a plurality of nanostructures of specific predetermined position, shape and composition, including nanostructure arrays having large area at high throughput necessary for industrial production. The resultant nanostructure patterns are useful for nanostructure arrays, specifically sensor and catalytic arrays

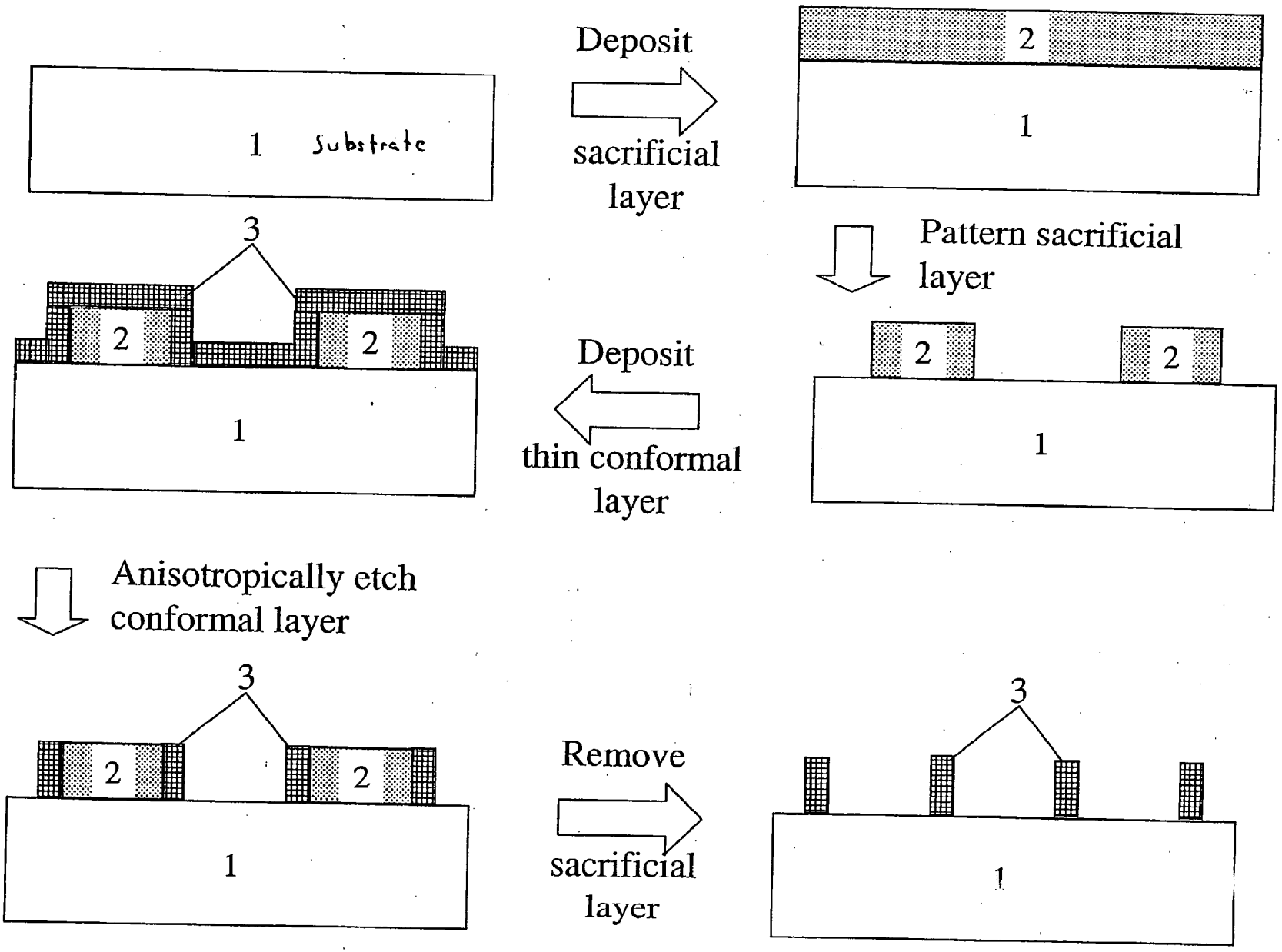

1 Substrate
Deposit
sacrificial layer
2
1
Pattern sacrificial layer
2
2
1
Deposit
thin conformal layer
3
2
2
1
Anisotropically etch conformal layer
3
2
2
1
Remove
sacrificial layer
3
1

FIG 1a

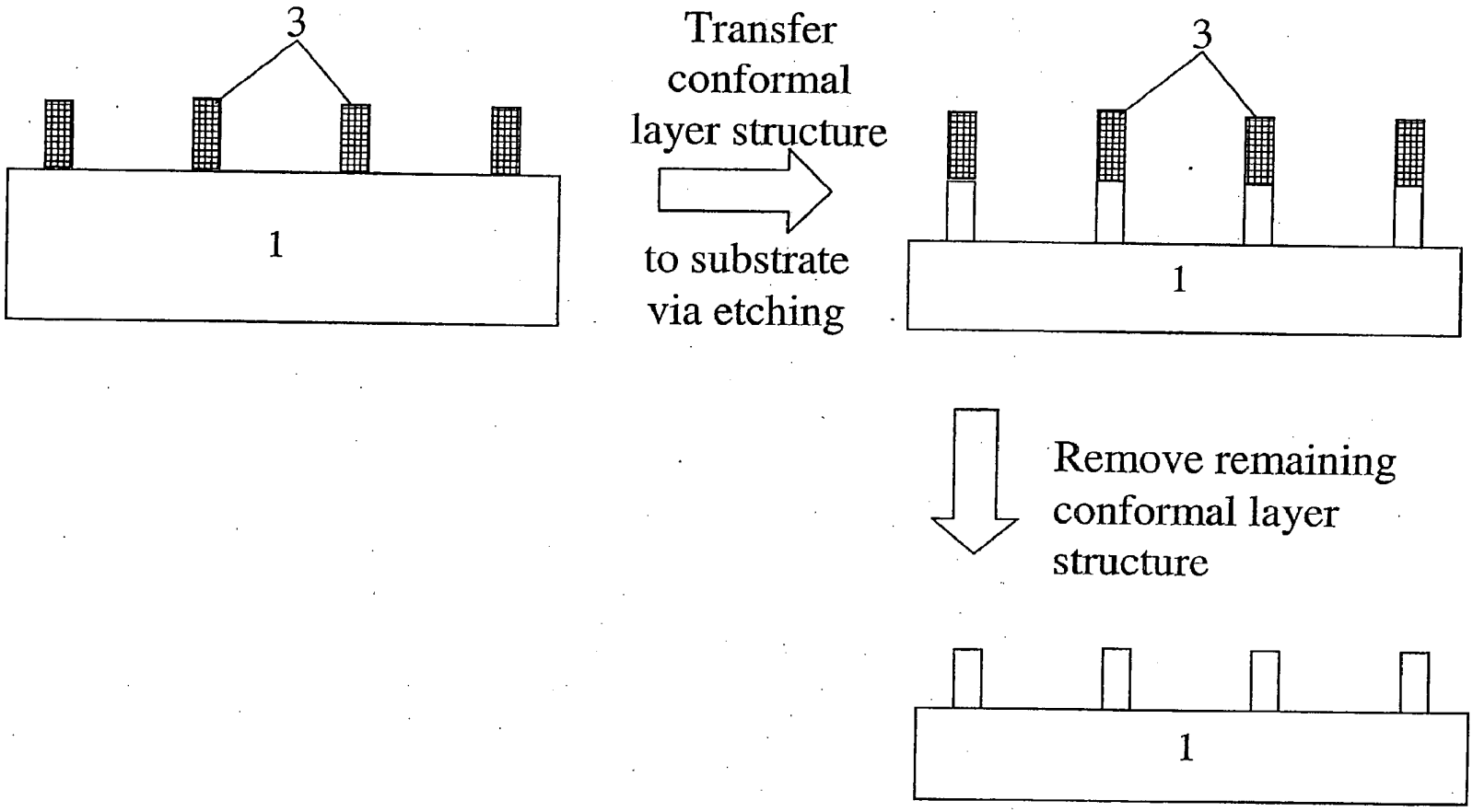

3
1
Transfer
conformal
layer structure
to substrate
via etching
3
1
Remove remaining
conformal layer
structure
1

FIG 16

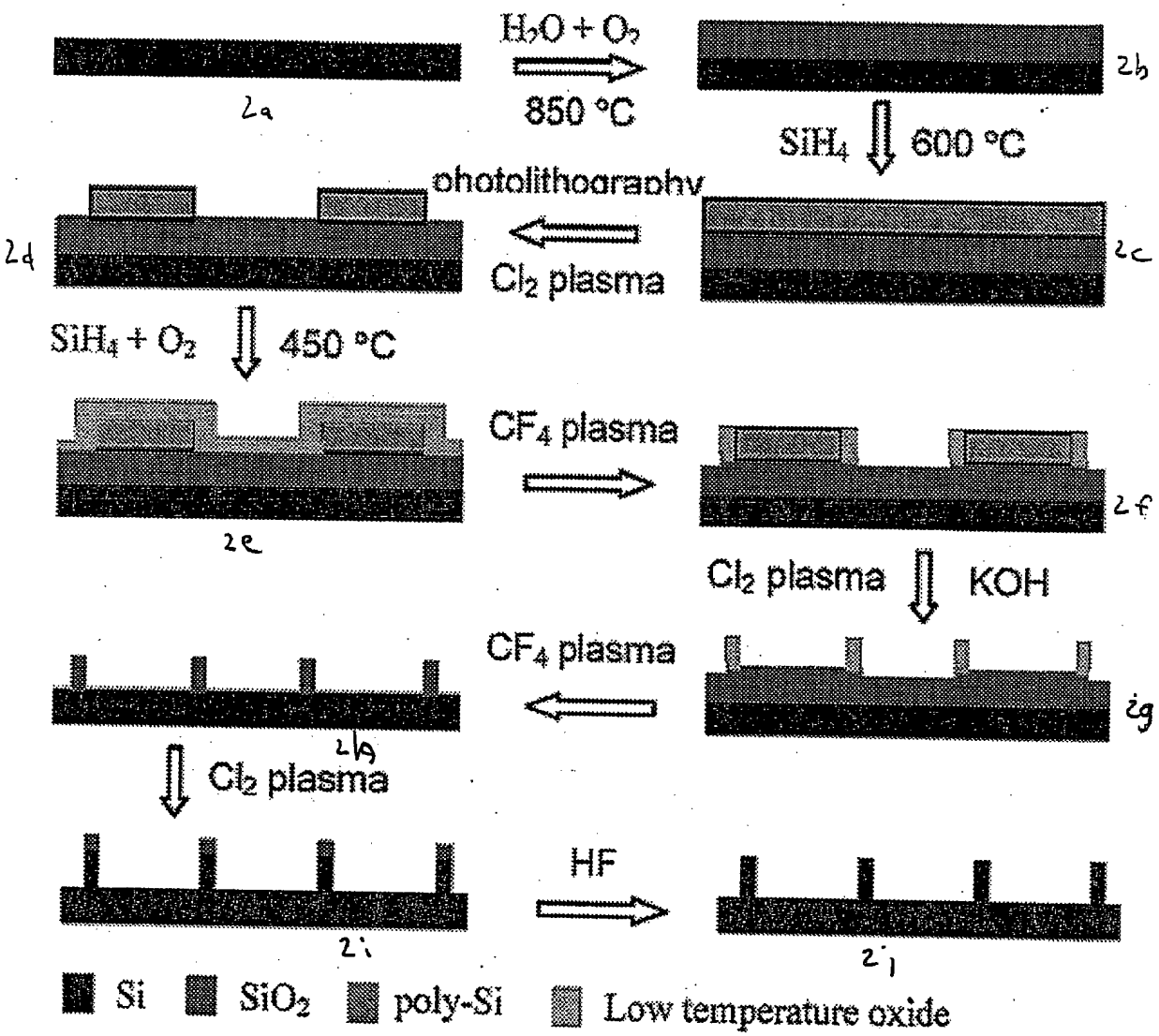

$H_2O + O_2$
850 °C
2a
2b
SiH_4 600 °C
photolithography
Cl_2 plasma
2d
2c
$SiH_4 + O_2$ 450 °C
CF_4 plasma
2e
2f
Cl_2 plasma
KOH
CF_4 plasma
2h
2g
Cl_2 plasma
HF
2i
2j
Si
SiO_2
poly-Si
Low temperature oxide

FIG 2a - 2j

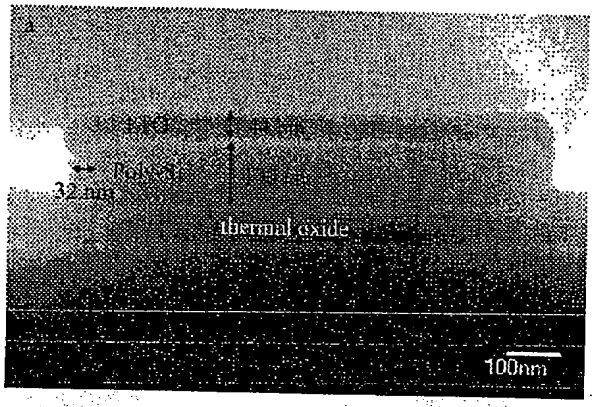

a
Poly-Si
32 nm
thermal oxide
100nm

FIG 3a

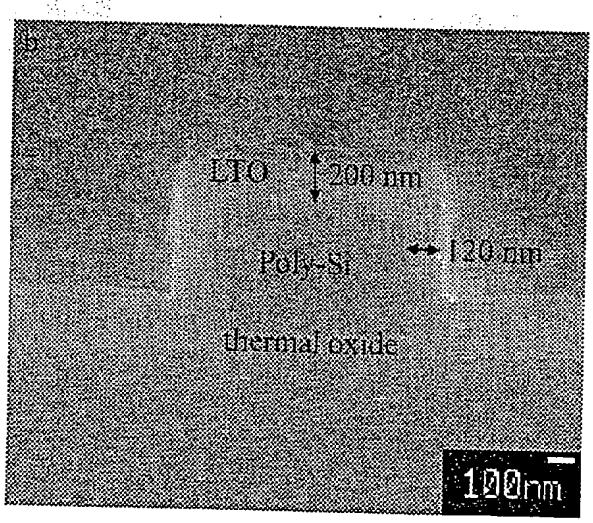

b
LTO
200 nm
Poly-Si
120 nm
thermal oxide
100nm

FIG 3b

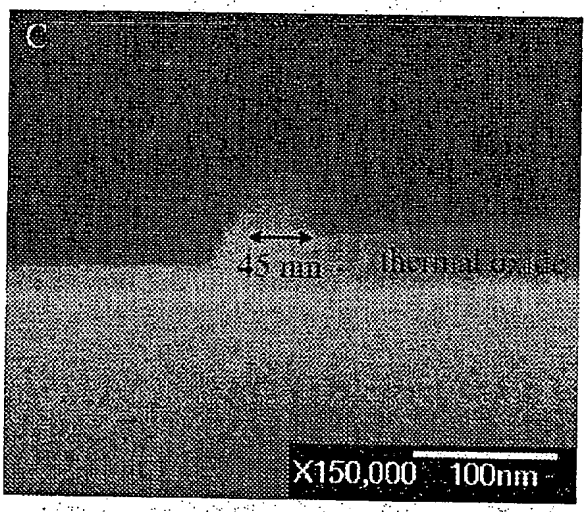


FIG 3c

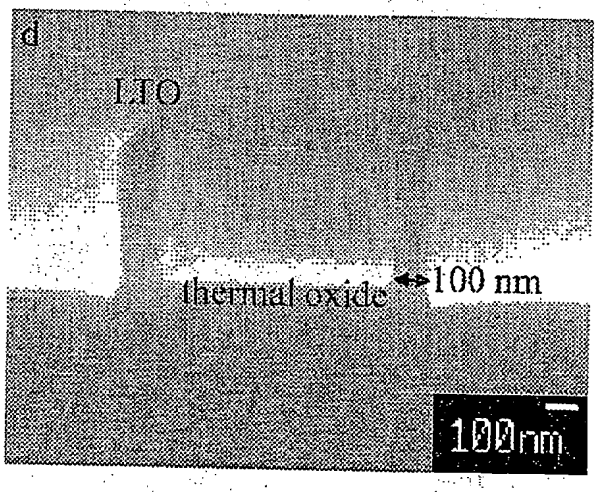


FIG 3d

10

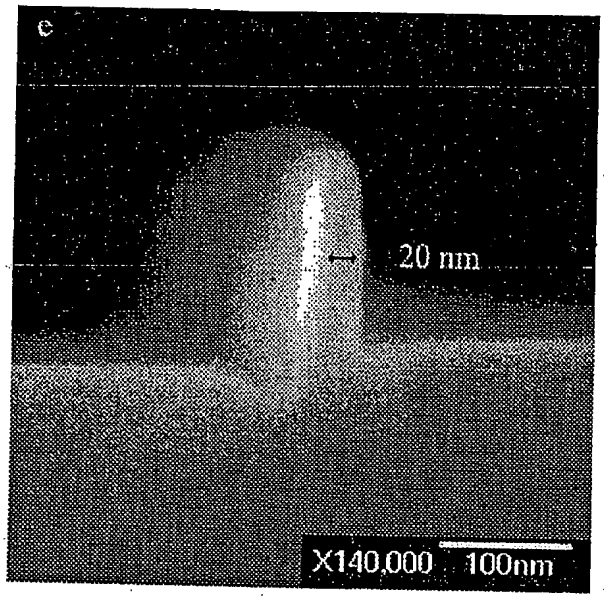


FIG 3e

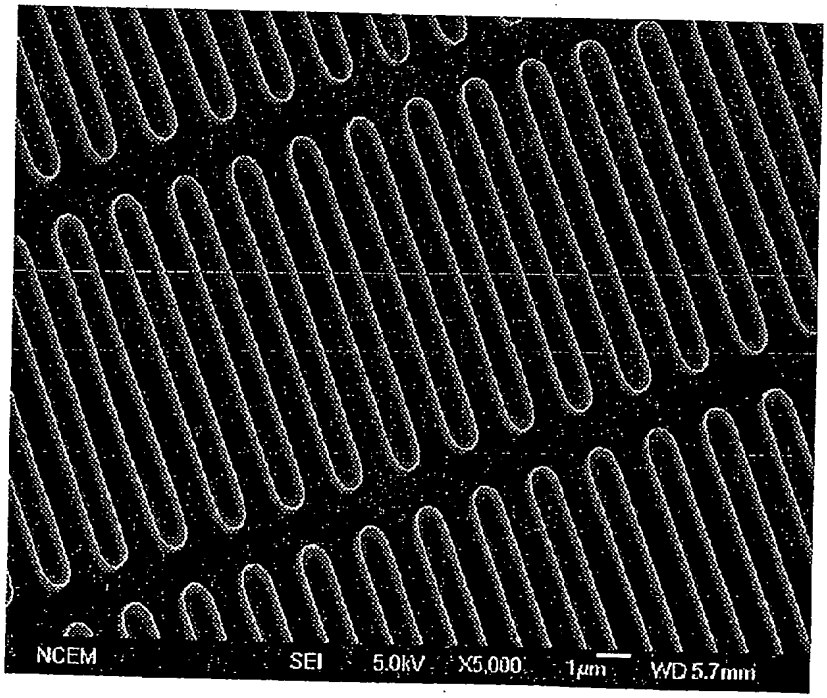


FIG 3f

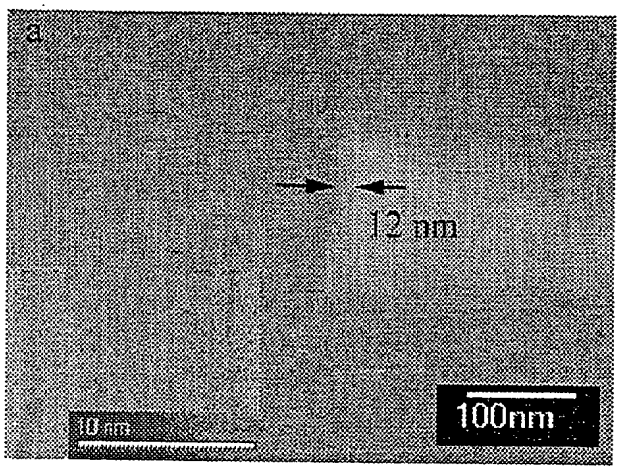


FIG 4a

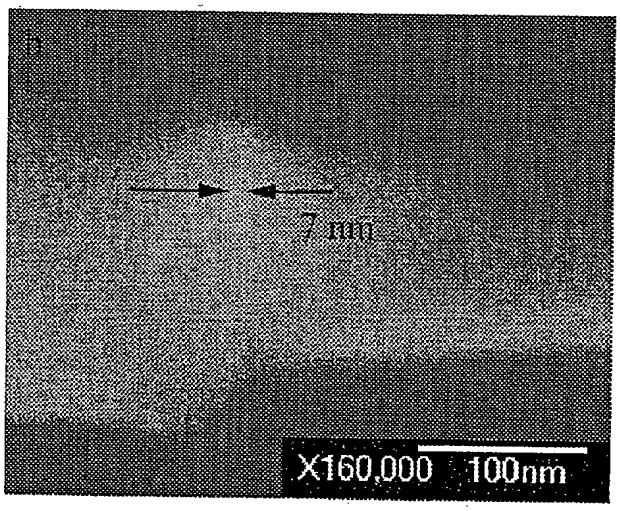


FIG 4b

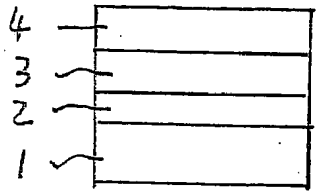


FIG 5a

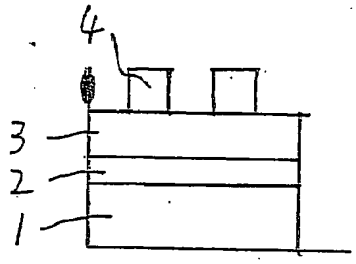


FIG 5b

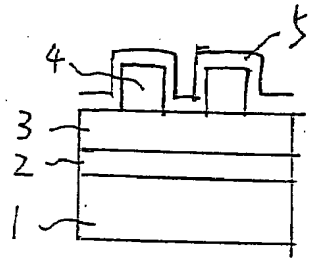


FIG 5c

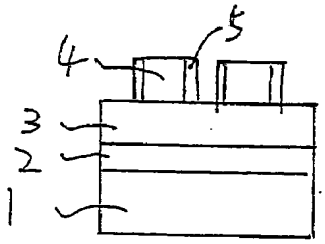


FIG 5d

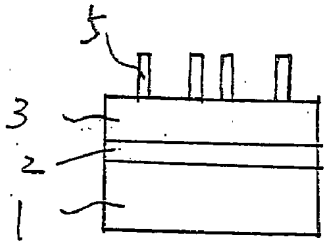


FIG 5e

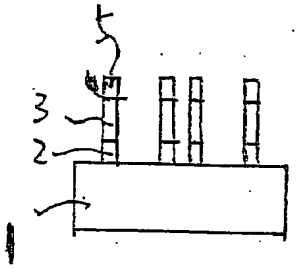


FIG 5f

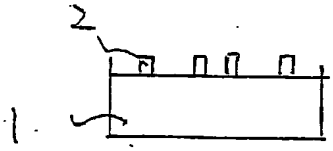


FIG 5g

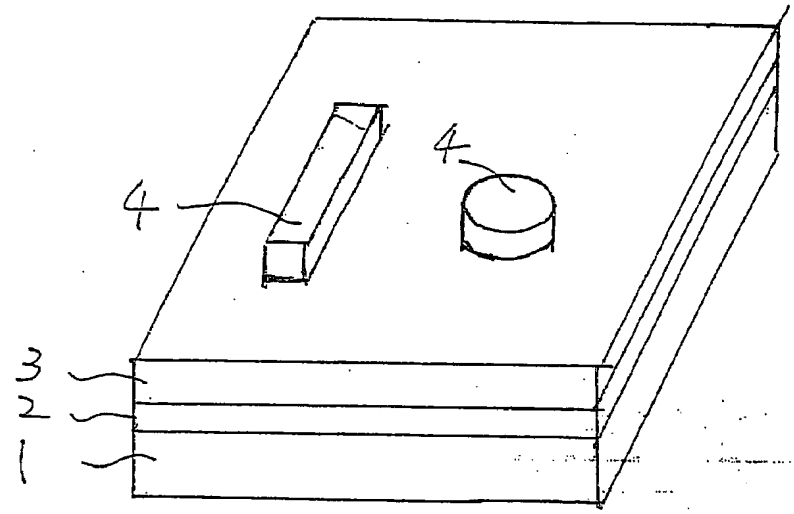


FIG 6a

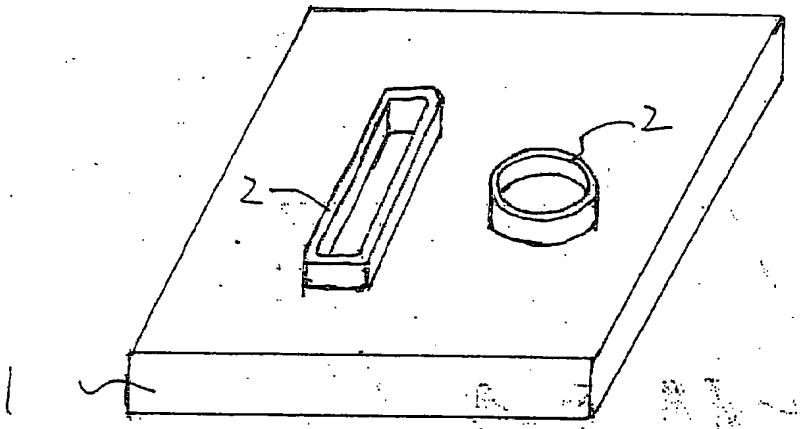


FIG 6b

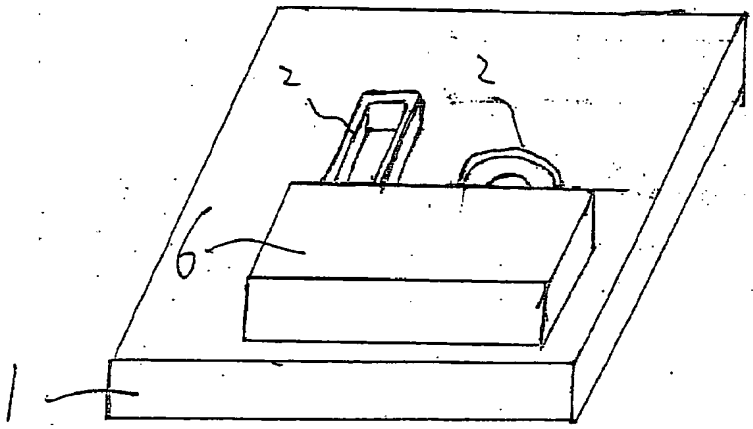


FIG 6c

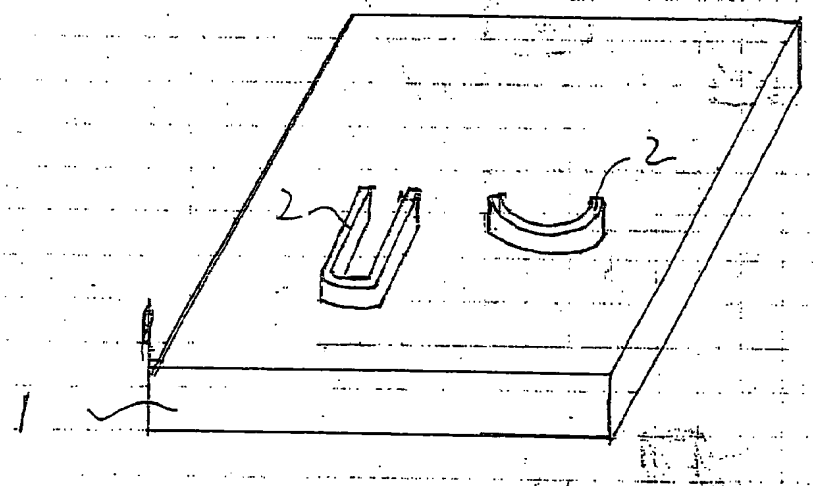


FIG 6d

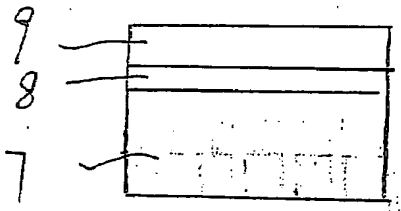


FIG 7a

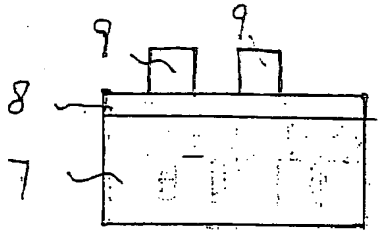


FIG 7b

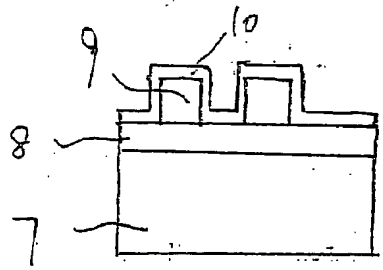


FIG 7c

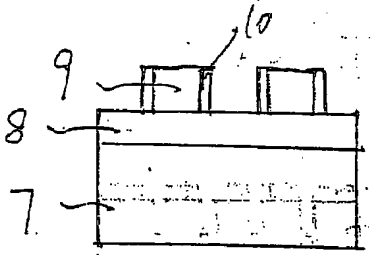


FIG 7d

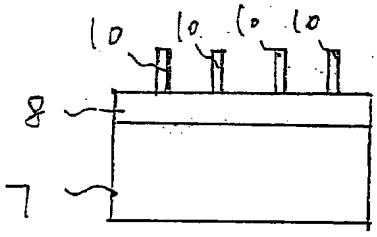


FIG 7e

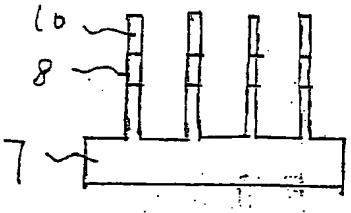


FIG 7f

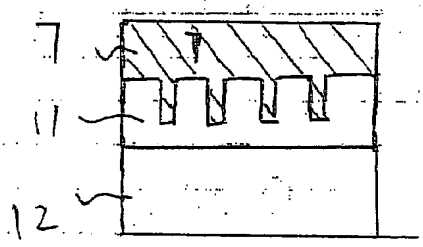


FIG 8a

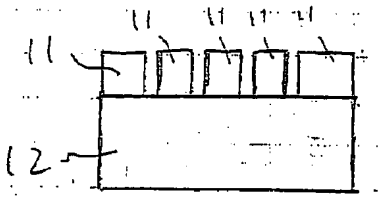


FIG 8b

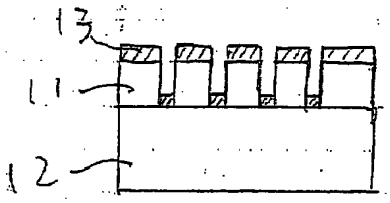


FIG 8c

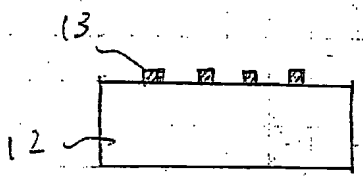


FIG 8d

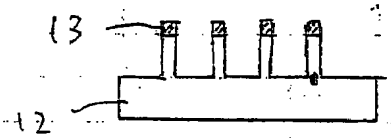


FIG 8e

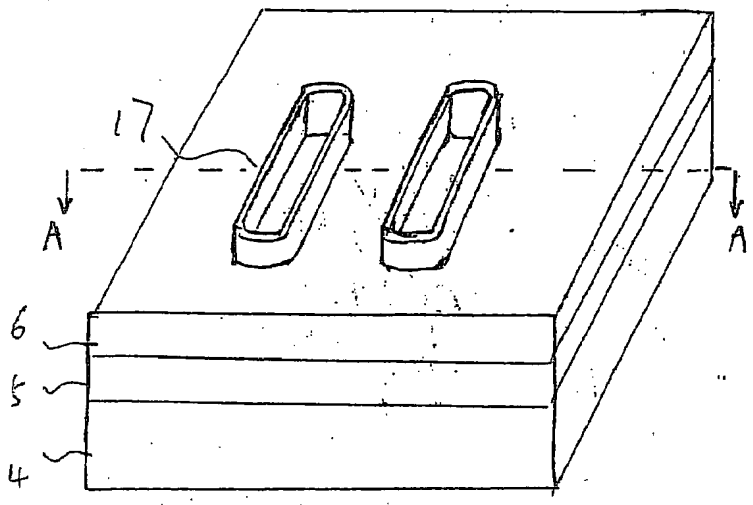


FIG 9a

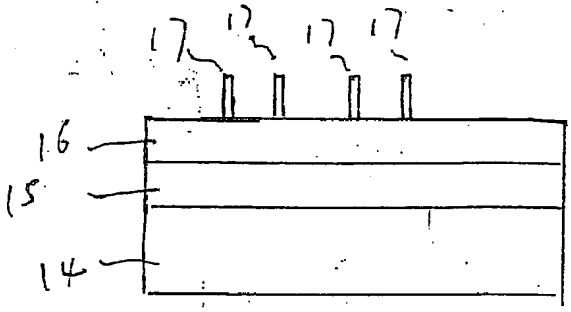


FIG 9b

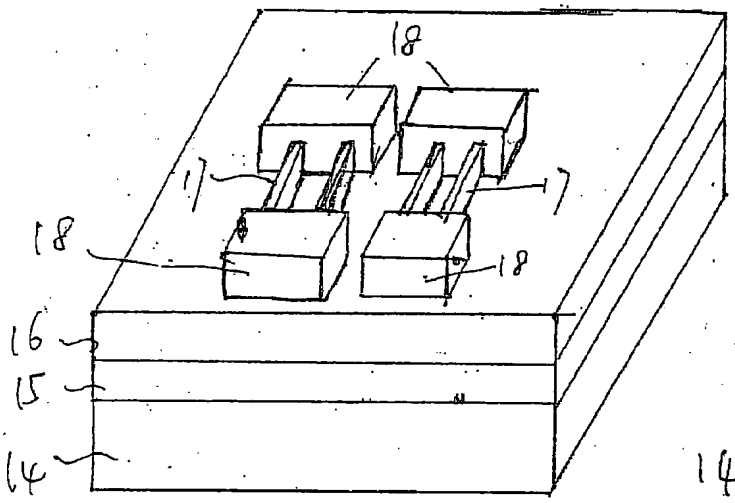


FIG 9c

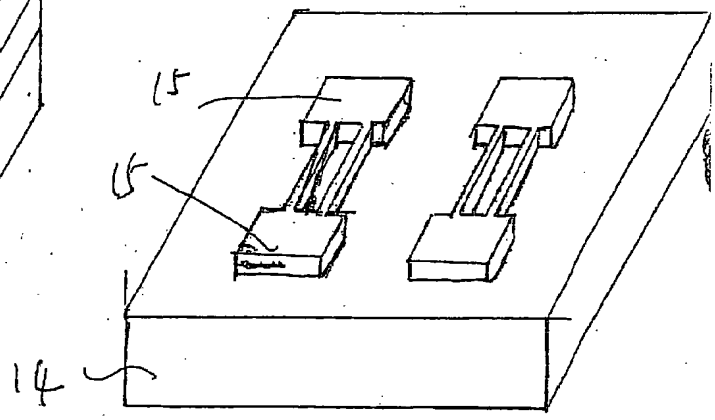


FIG 9d

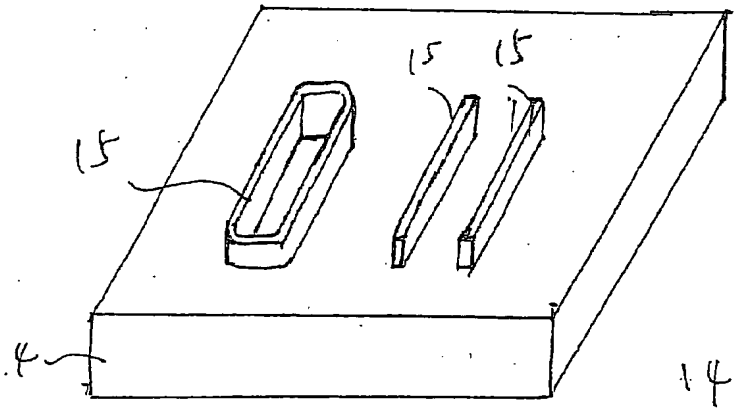


FIG 9e

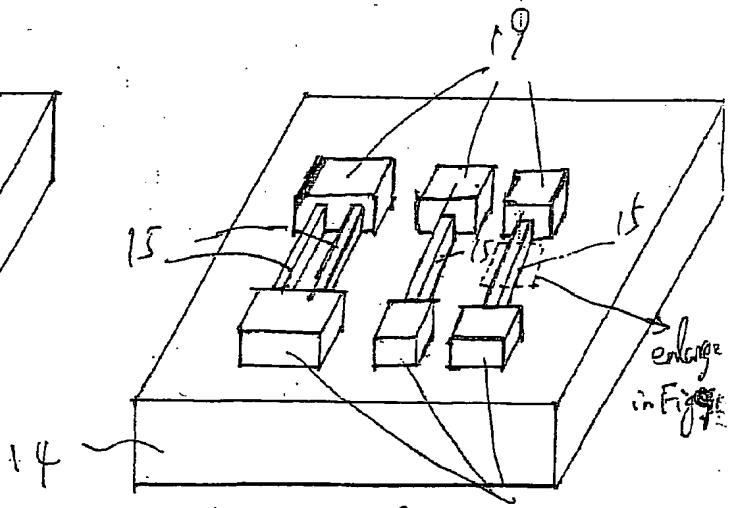


FIG 9f

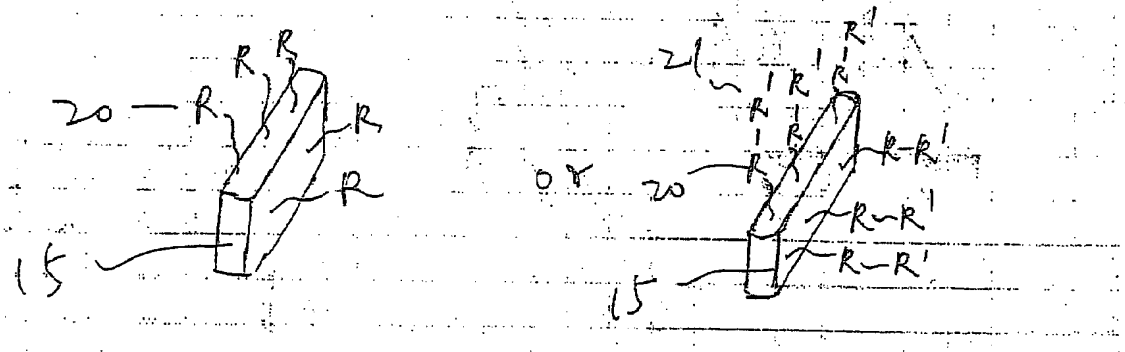


FIG 9g

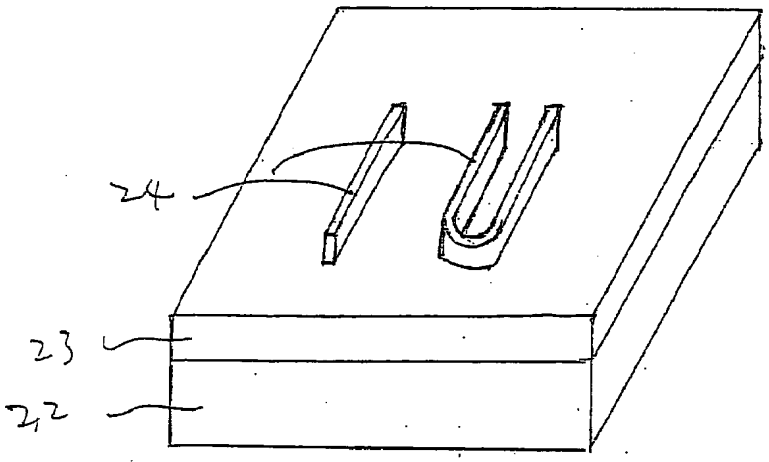


FIG 10a

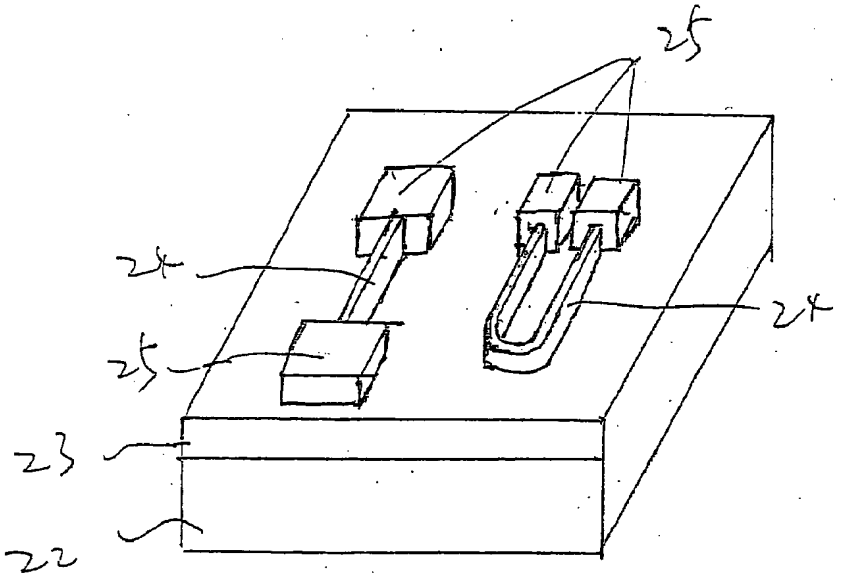


FIG 10b

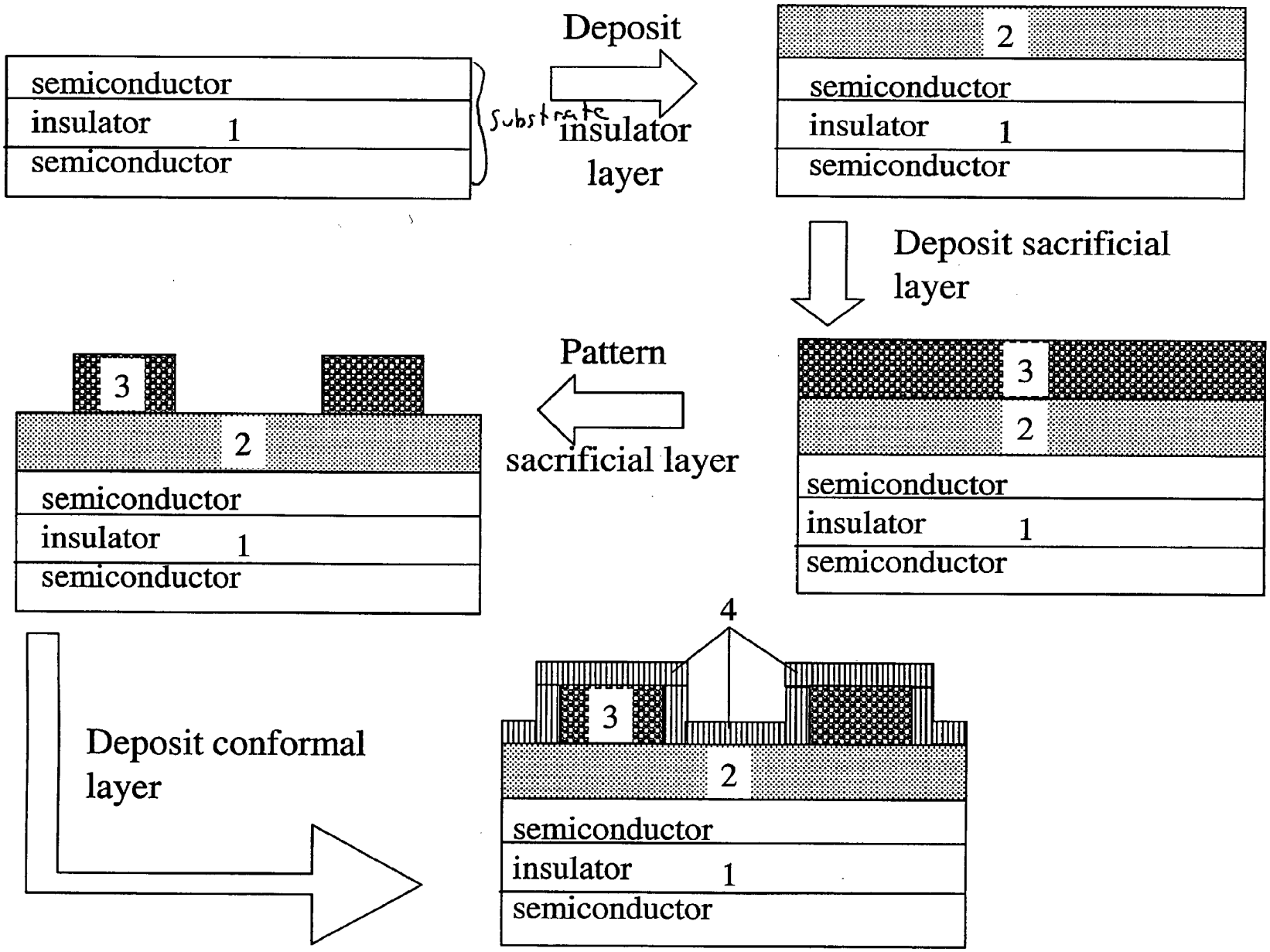

semiconductor
insulator 1
semiconductor
Substrate
Deposit
insulator layer
2
semiconductor
insulator 1
semiconductor
Deposit sacrificial layer
3
2
semiconductor
insulator 1
semiconductor
Pattern
sacrificial layer
3
2
semiconductor
insulator 1
semiconductor
Deposit conformal layer
4
3
2
semiconductor
insulator 1
semiconductor

FIG 11

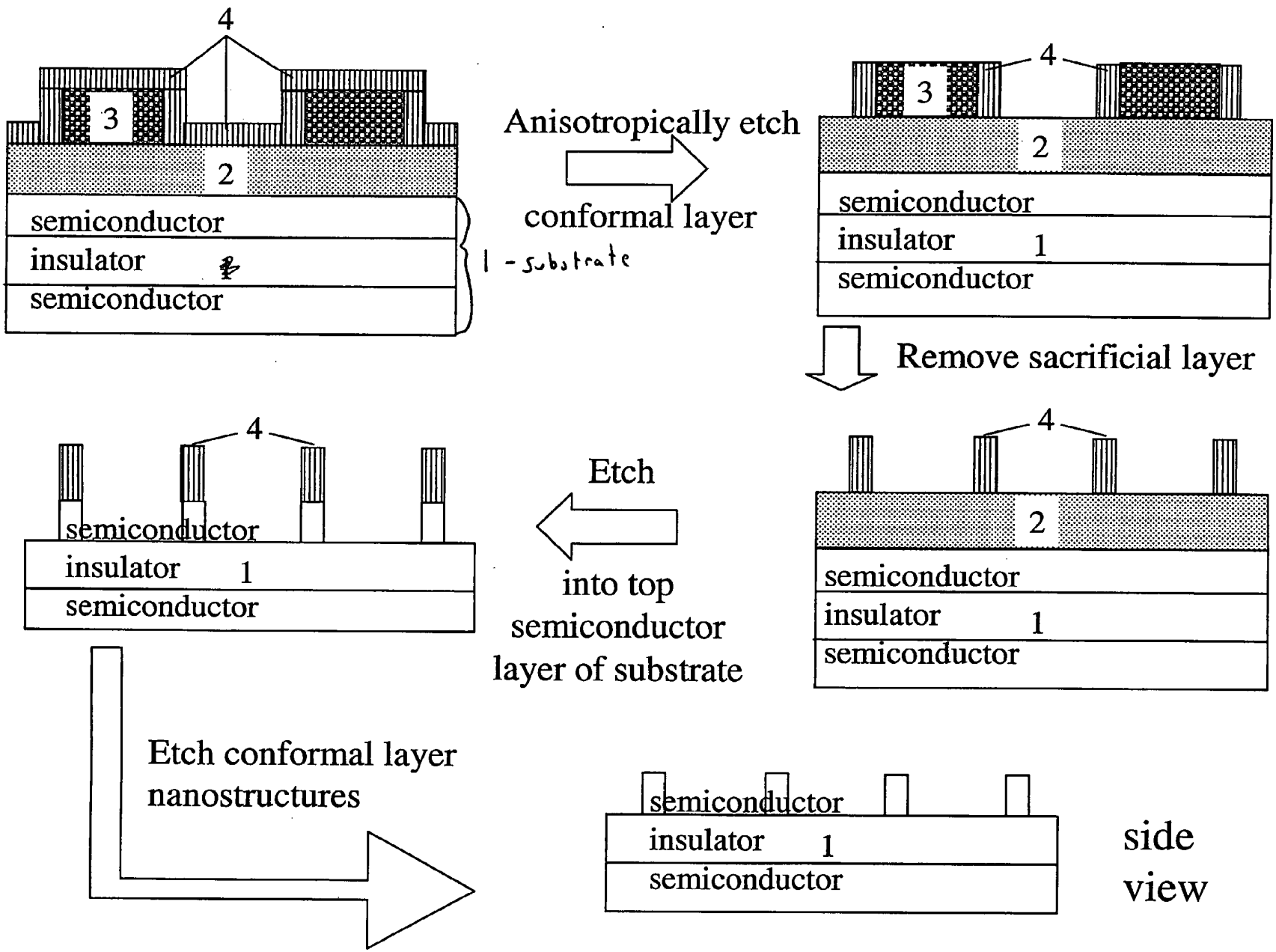

4
3
2
semiconductor
insulator
semiconductor
1 - substrate
Anisotropically etch
conformal layer
4
3
2
semiconductor
insulator 1
semiconductor
Remove sacrificial layer
4
2
semiconductor
insulator 1
semiconductor
Etch
into top
semiconductor
layer of substrate
4
semiconductor
insulator 1
semiconductor
Etch conformal layer
nanostructures
semiconductor
insulator 1
semiconductor
side
view

FIG 12

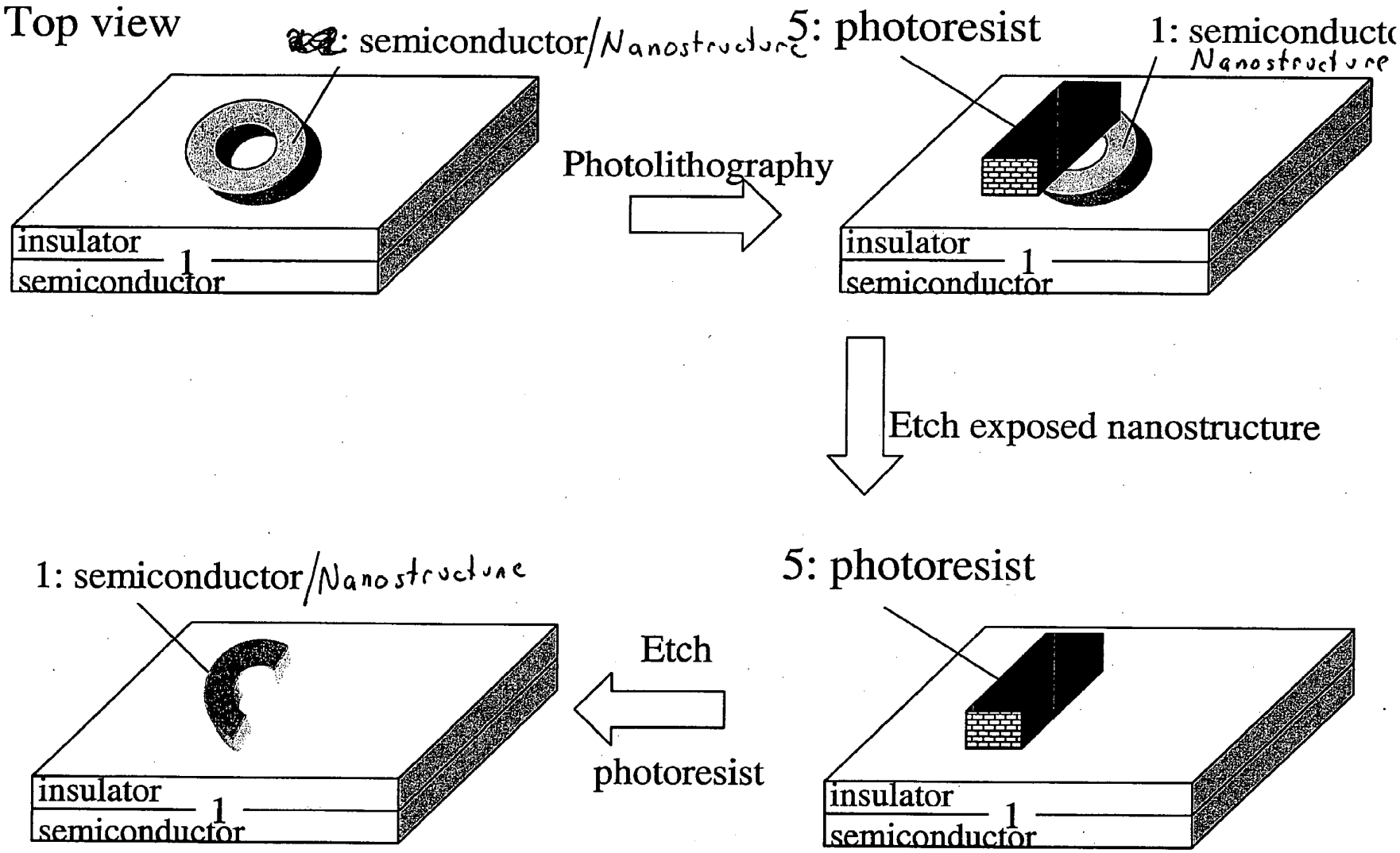

Top view
1: semiconductor/Nanostructure
5: photoresist
1: semiconducto
Nanostructure
Photolithography
insulator
1
semiconductor
insulator
1
semiconductor
Etch exposed nanostructure
1: semiconductor/Nanostructure
5: photoresist
Etch
photoresist
insulator
1
semiconductor
insulator
1
semiconductor

FIG 13

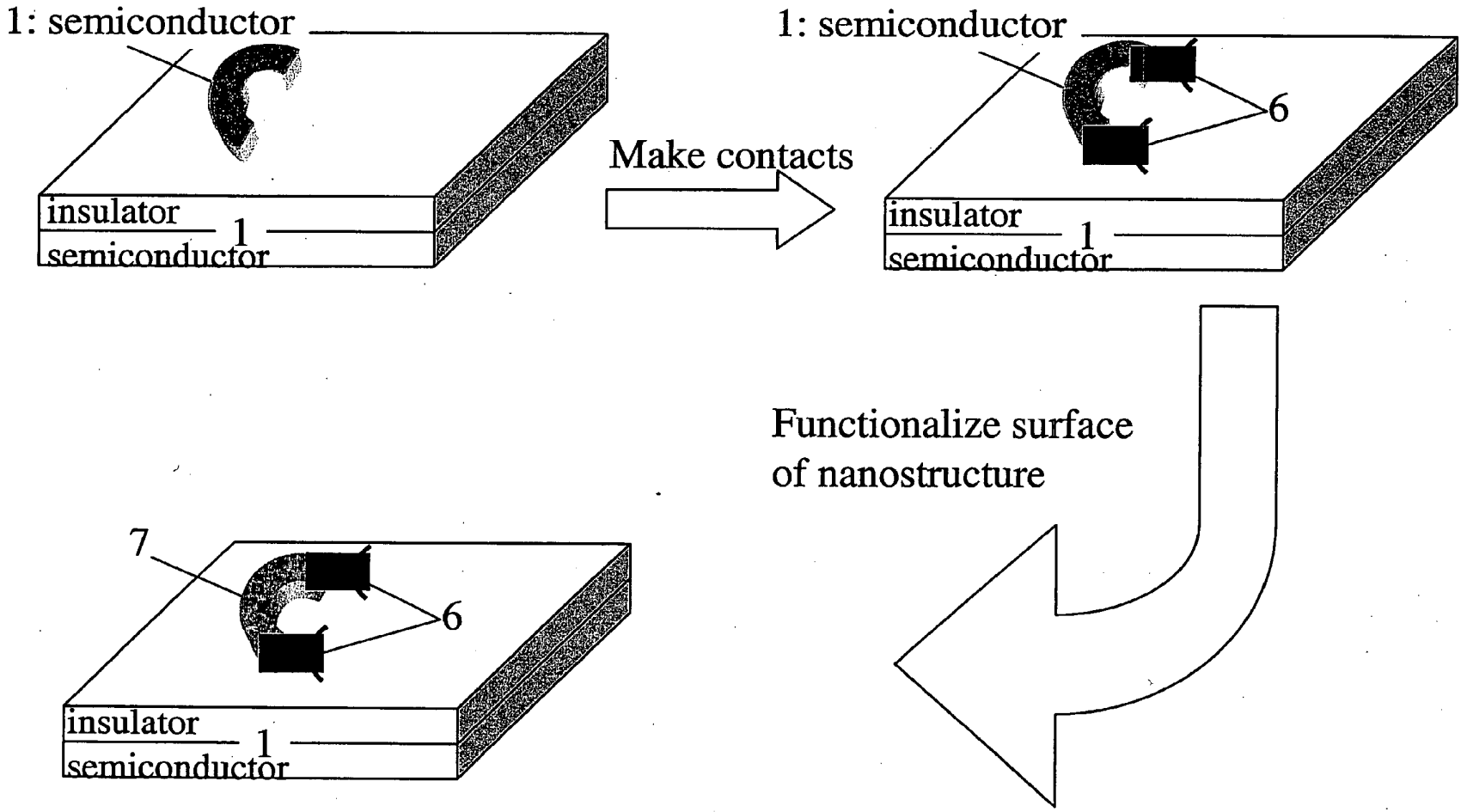

1: semiconductor
insulator
1
semiconductor
Make contacts
1: semiconductor
6
insulator
1
semiconductor
Functionalize surface
of nanostructure
7
6
insulator
1
semiconductor

FIG 14

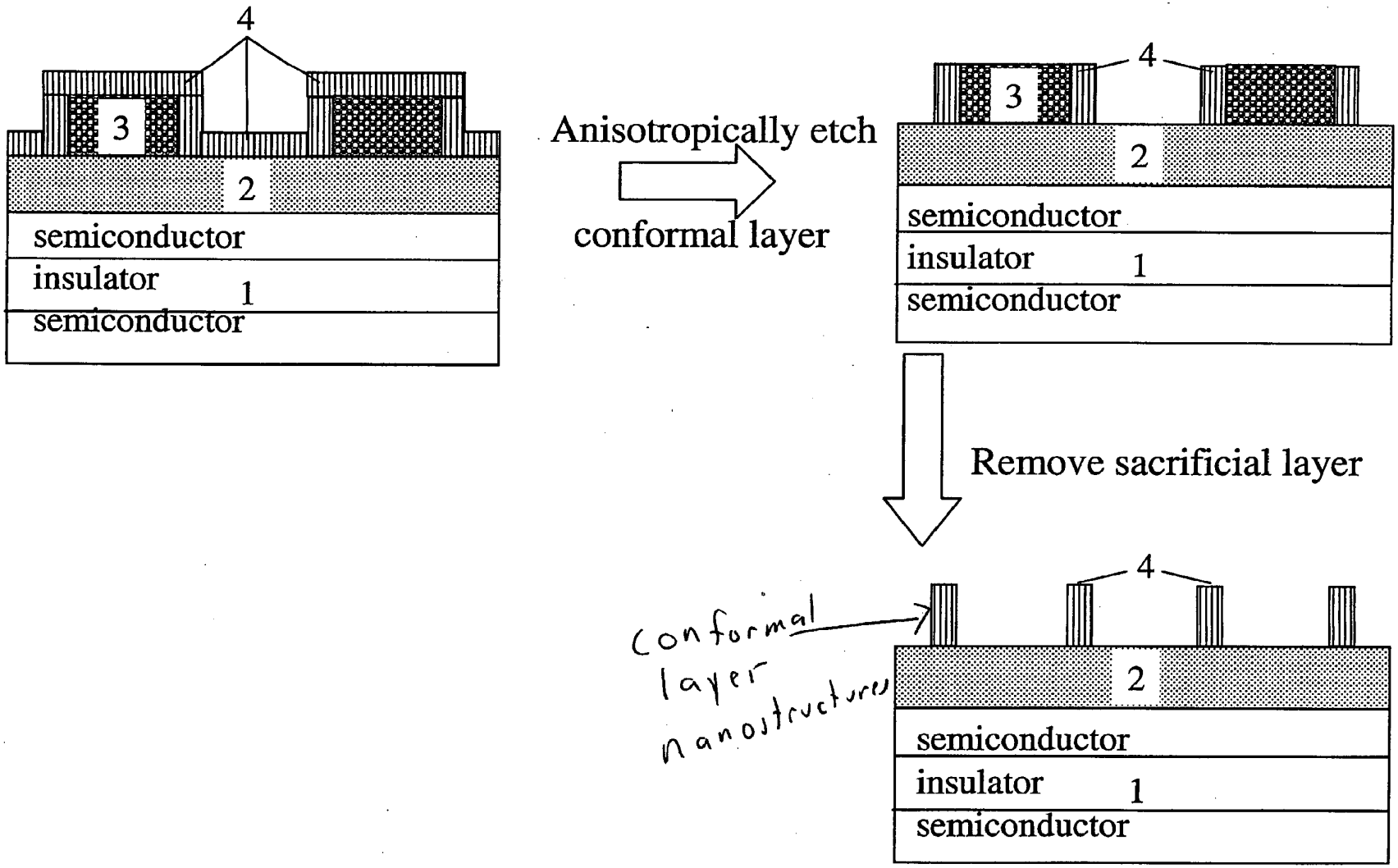

4
3
2
semiconductor
insulator
1
semiconductor
Anisotropically etch
conformal layer
4
3
2
semiconductor
insulator
1
semiconductor
Remove sacrificial layer
conformal layer nanostructures
4
2
semiconductor
insulator
1
semiconductor

FIG 15

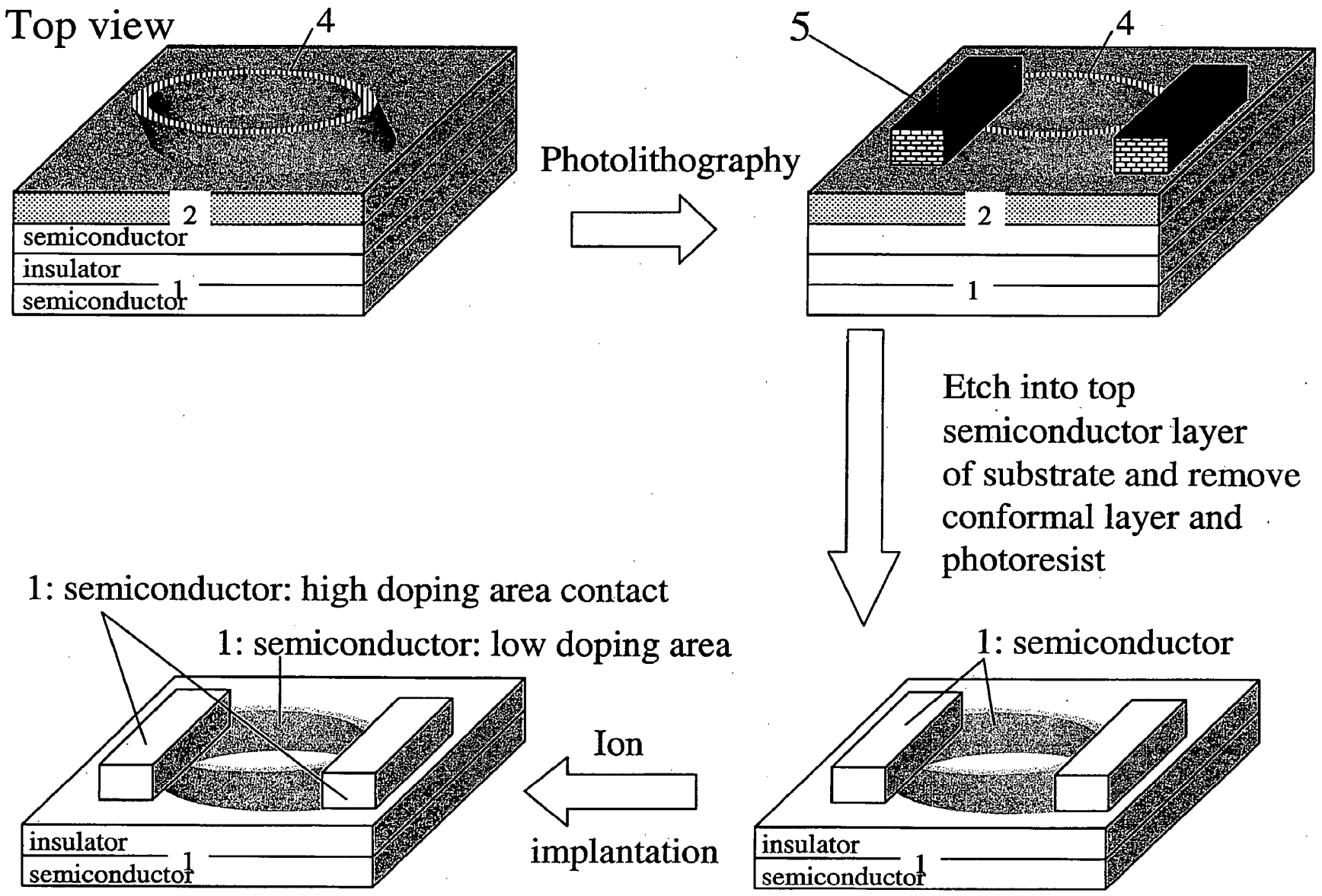

Top view
4
2
semiconductor
insulator
semiconductor
1
Photolithography
5
4
2
1
Etch into top semiconductor layer of substrate and remove conformal layer and photoresist
1: semiconductor
insulator
semiconductor
1
Ion implantation
1: semiconductor: high doping area contact
1: semiconductor: low doping area
insulator
semiconductor
1

FIG 16

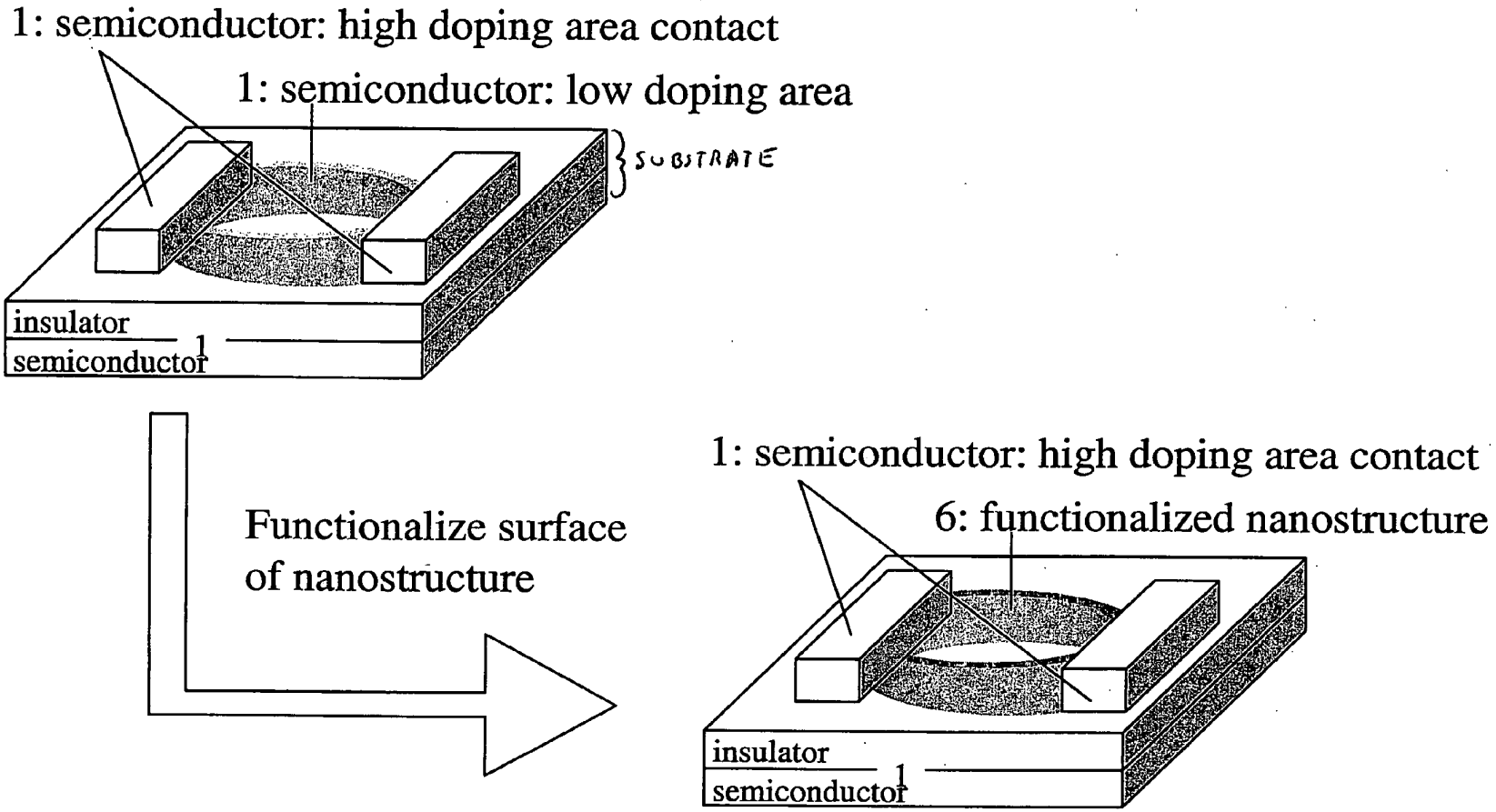

1: semiconductor: high doping area contact
1: semiconductor: low doping area
SUBSTRATE
insulator
semiconductor
1
Functionalize surface
of nanostructure
1: semiconductor: high doping area contact
6: functionalized nanostructure
insulator
semiconductor
1

FIG 17

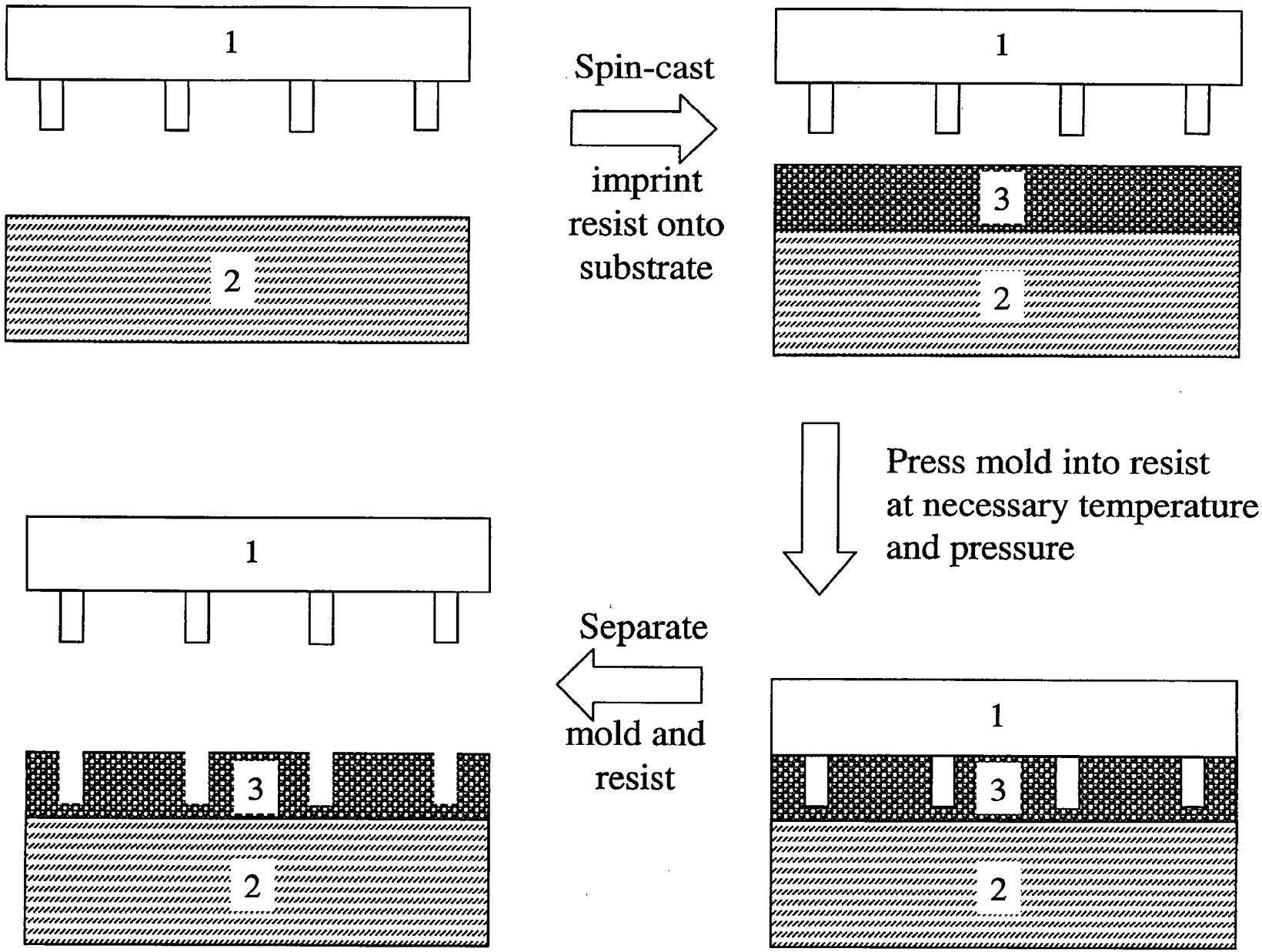

1
2
Spin-cast
imprint
resist onto
substrate
1
3
2
Press mold into resist
at necessary temperature
and pressure
1
3
2
Separate
mold and
resist
1
3
2

FIG 18

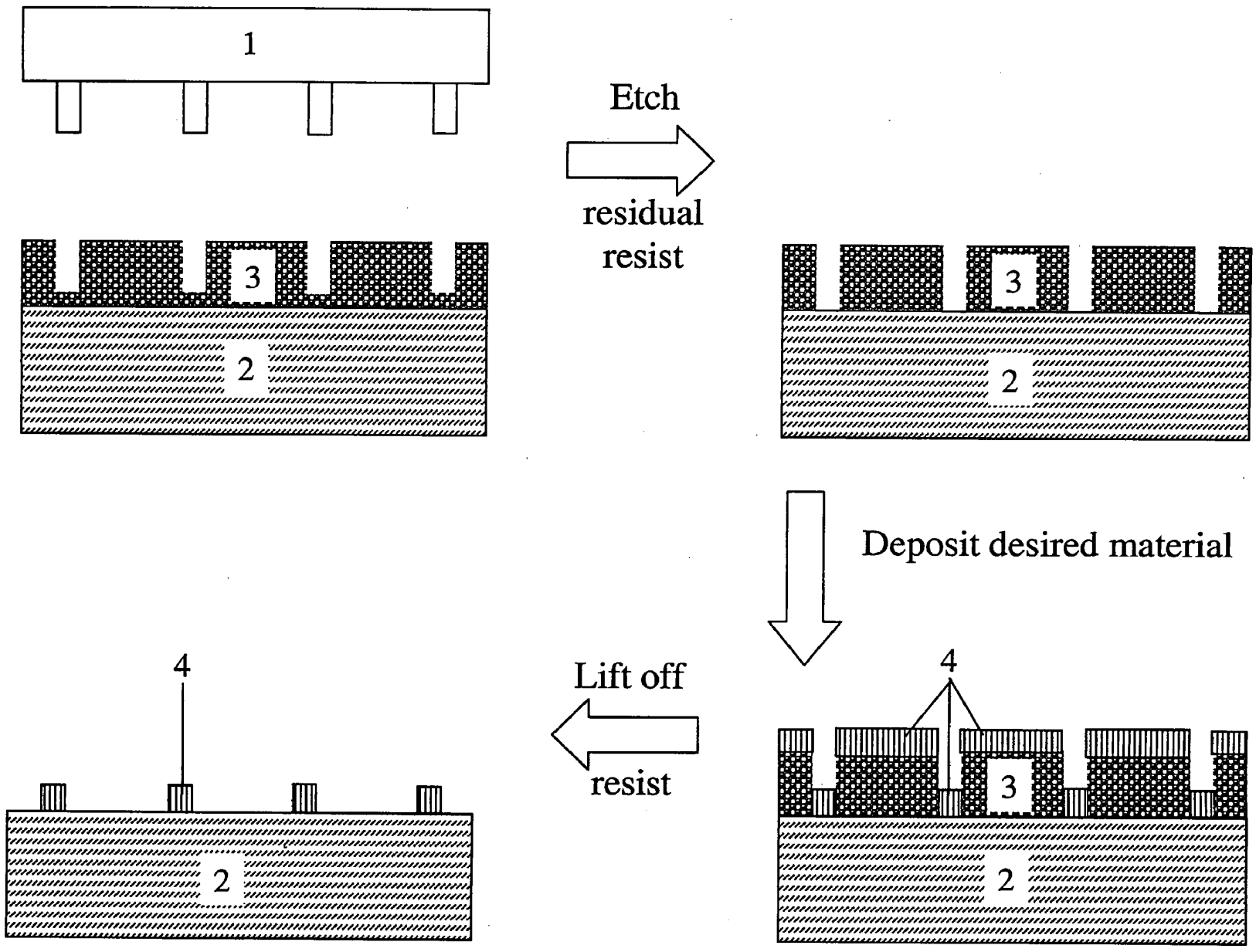
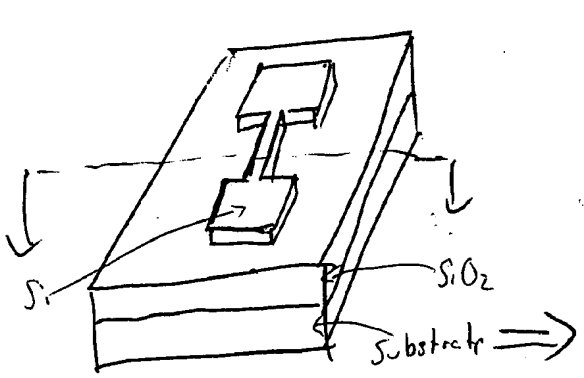

1
Etch
residual
resist
3
2
3
2
Deposit desired material
4
4
Lift off
resist
3
2
2

FIG 19



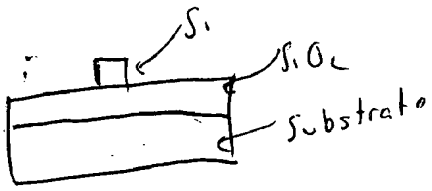
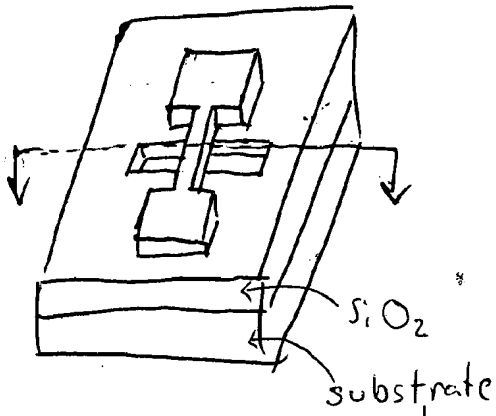


FIG 20a



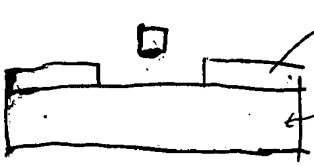


FIG 20b